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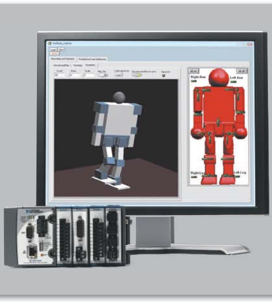

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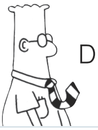

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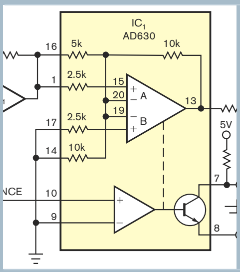

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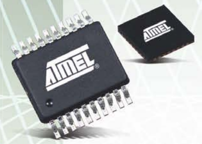

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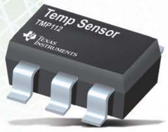

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ONLINE ONLY

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Taking power analysis to the transistor level for a full chip

Neither functional simulation nor conventional power estimation can catch some major issues in power consumption for low-power designs. Large-area mixed-signal simulation may be the right answer.

→www.edn.com/article/CA6709857

SEE NAKED ICs

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BY RON WILSON, EXECUTIVE EDITOR

Semiconductors, emerging markets, and the self-interest of survival

Some time ago, as the storm of recession broke over the industry, I opined that companies should look quickly to developing markets for demand that was not based on conspicuous consumption. Since then, a devastating collapse in end-user demand has occurred across the industrialized nations. In contrast, countries such as China and India appear to be using their banks to support their citizenry—rather than committing ordinary citizens to enrich the banks. These actions seem to justify my dim view of developed-world demand.

Apparently, European companies—always of necessity more outward-looking than their US competitors—are starting to believe similarly. According to a recent *Financial Times* article, companies including electronics manufacturer Philips, car maker Renault, and German truck-builder MAN are planning to get more than half their sales from emerging markets by 2015 (**Reference 1**). According to electrical-engineering giant ABB, 55% of new orders in the third quarter of this year came from emerging markets.

The *Financial Times* article also quotes David Michael, head of Boston Consulting Group's globalization practice in Beijing. "Many industries are at the tipping point where 50% or more of global demand is in emerging markets," he says. There is a simple message here. If your business plan is to be part of a supply chain that ultimately brings expensive discretionary goods to developed markets, you have a short-term problem rapidly turning into a long-term strategic error. You are specializing away from the market growth.

It is simple arithmetic. As Xilinx President and Chief Executive Officer Moshe Gavrielov points out, a genuine and growing end-user demand is coming from people around the world—people who perhaps for the first time can make discretionary purchases. Accordingly, market growth in today's world will come disproportionately from emerging economies, in which huge numbers of formerly destitute people are finally achieving a bit of disposable income. They will spend this income on quality-of-life and livelihood-supporting purchases, such as cell phones, appliances, and safe transportation. Proportionately less growth will come from the developed world, which already lost its credit and in which the aging population is losing its acquisitiveness as older people gradually stop buying stuff.

For companies that have lived in the lifestyle supply chain, however, change is complex. It requires learning what life is like for the emerging middle class. And change means learning how investment patterns in emerging economies turn into demand for electronics systems and, ultimately, for semiconductors. That learning must come by working with emerging-market system OEMs and service providers that are already successful in their local markets. The *Financial Times* article says that major competition for the Europeans' expansion would come not from US companies but from local ones, such as Shanghai Electric and Huawei. Finally, it means innovating to drastically reduce product cost in competitive markets, rather than firing people to incrementally reduce fixed expenses.

Looking outward, understanding countries' development plans and their people's lives, partnering across cultural boundaries, and creating instead of copying comprise a kind of humanitarianism that has nothing to do with charity. For US semiconductor companies, it is about survival.**EDN**

REFERENCE

1. Milne, Richard, "Ambitious growth targeted as groups look to fresh territories," *Financial Times*, Nov 20, 2009, www.ft.com/cms/s/0/cdf8da30-d573-11de-81ee-00144feabdc0.html?nclick_check=1.

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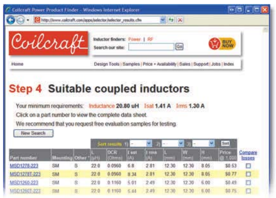

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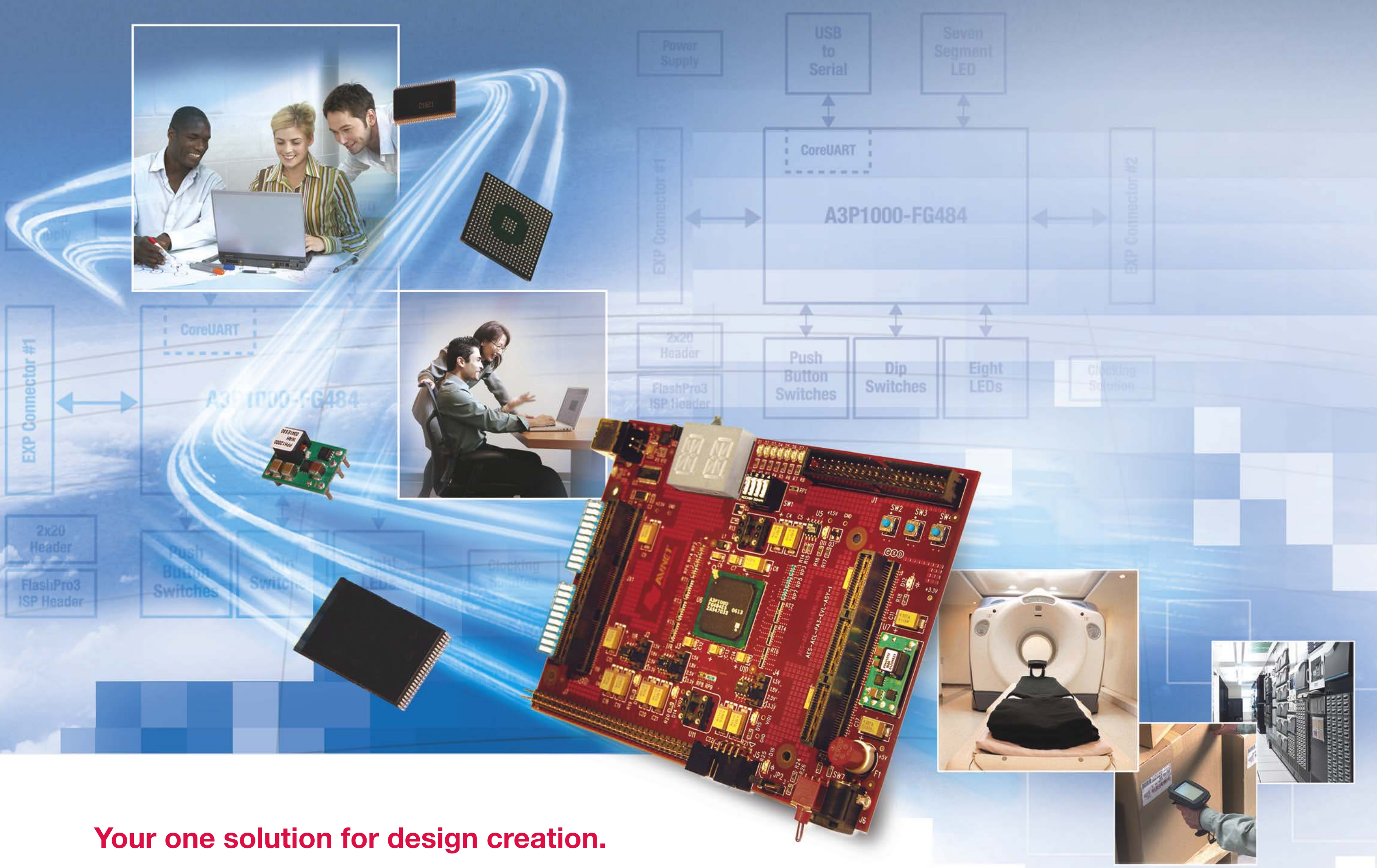

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EDITED BY FRAN GRANVILLE

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INNOVATIONS & INNOVATORS

Power supplies for new LED applications fit into high-margin markets

IC vendors eagerly anticipate that the huge market for LED bulbs to replace incandescent and CFL (compact-fluorescent-light) bulbs will drive the demand for ac/dc power-management ICs. The largest bulb-replacement market of all, the replacement of 60W light bulbs, will have razor-thin profit margins and most likely go straight to Asian manufacturers. As a result, signage, displays, and industrial lighting may be more promising markets for US companies focusing on high-power-LED designs.

For example, the Mitsubishi Electric (www.mitsubishielectric.com) screen at the Dallas Cowboys' Cowboys Stadium uses 22,000 TDK-Lambda ZWS100AF-5-series power supplies to drive more than 20 million LEDs. Digi-Key (www.digikey.com) lists the supplies at $20 (100). Lambda also recently released the LD12 series of ac/dc power supplies for LED-lighting and -display applications, offering as much as 12.6W of power and with both constant-voltage and constant-current models available. The encapsulated devices operate with universal power inputs of 90 to 265V ac. The constant-voltage LDV12 series comes with 12, 15, or 24V outputs; the $14.50 (1000) LDC12 constant-current units provide 350 to 750 mA with dc-output ranges of 3 to 18 or 3 to 36V. Typical output efficiencies are 82% under full load.

Another promising, albeit more mundane, market for external power supplies is industrial lighting with LEDs. For example, Power Partners introduced its PIL100 series of 100W ac/dc LED-lighting power modules, also with a choice of constant-current or constant-voltage models. All models accept as much as 305V ac; the output on the constant-current models is 350 to 4200 mA, and the constant-voltage models offer 12 to 105V-dc outputs. Efficiency is as high as 93%.

—by Margery Conner

▷**TDK-Lambda**, www.tdk-lambda.com.
▷**Power Partners**, www.powerpartners-inc.

FEEDBACK LOOP

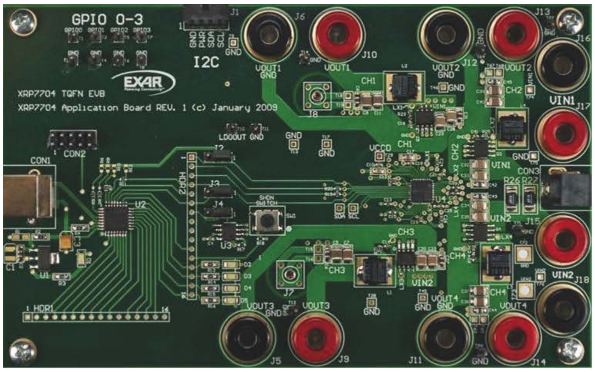
"Success has many parents, but a knotty problem is an orphan."

—Software engineer JT Klopcic, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6705270. Add your comments.

Mitsubishi Electric claims that the video-screen system for the Dallas Cowboys' Cowboys Stadium includes the world's largest high-definition video display with two 160×72-foot sideline displays, each using more than 10 million LEDs.

Quad-PWM-controller IC includes low-dropout linear regulator

Exar Corp's new 5A XRP7704 and 16A XRP7740 quad-PWM (pulse-width-modulation)-controller chips include gate-driver circuitry that drives external FETs. In addition to the four PWM voltage regulators, the devices include a low-dropout linear regulator, which you can use for auxiliary or standby power. The input-voltage range is 6.5 to 20V, and you can set the output voltages at 0.9 to 5V. The four PWM outputs have 12-bit resolution, and the units, which you can program through an I^2C (inter-integrated-circuit) interface, have six general-purpose digital-I/O pins. They use a digital PID (proportional/integral/differential) algorithm that tailors control-loop response up to a 1.5-MHz switching frequency.



The Exar XRP7704 demo board allows you to evaluate the performance and characteristics of this quad-output controller.

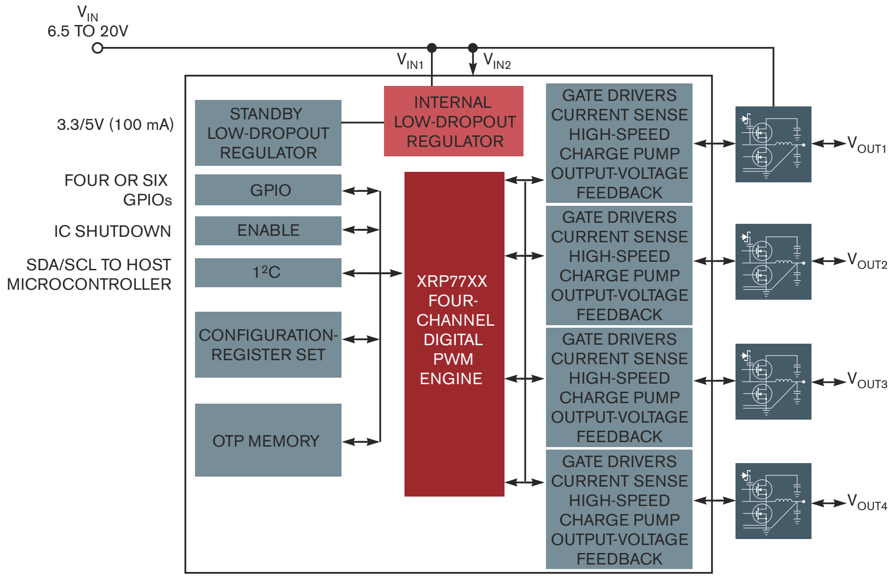
Applications include POL (point-of-load) dc/dc power conversion in high-volume and cost-sensitive consumer devices, such as set-top boxes, and industrial markets, such as servers and instrumentation. The units store their settings in OTP (one-time-programmable) memory, but your system processor can overwrite those settings using the I^2C bus.

The Digital Power Studio software environment allows you to program and communicate with the chips as you develop your power system. The package lets you configure the power supply's voltage settings, current thresholds, fault monitoring and response, soft start, shutdown, channel sequencing, phase-shift management, and loop response. You can also control the parts in real time using the I^2C port with your system microcontroller, FPGA, or ASIC. You can configure as many as eight PWM controllers by linking two parts together in a master/slave arrangement.

Both parts come in 40-pin QFN packages, comply with ROHS (reduction-of-hazardous-substances) directives, operate at −40 to +85°C, and are available for sampling. The XRP7704 sells for $4; the XRP7740 sells for $5.50 (1000).**—by Paul Rako**

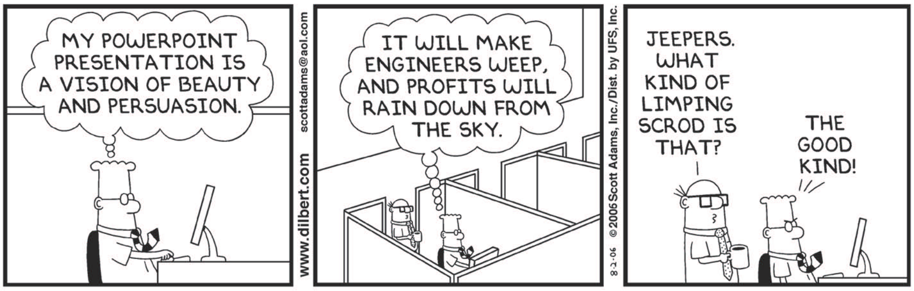
▷**Exar Corp**, www.exar.com.

> The Digital Power Studio allows you to program and communicate with the chips as you develop your power system.



The XRP7704 has four PWM controllers, a low-dropout linear regulator, and drivers for external FETs.

DILBERT By Scott Adams

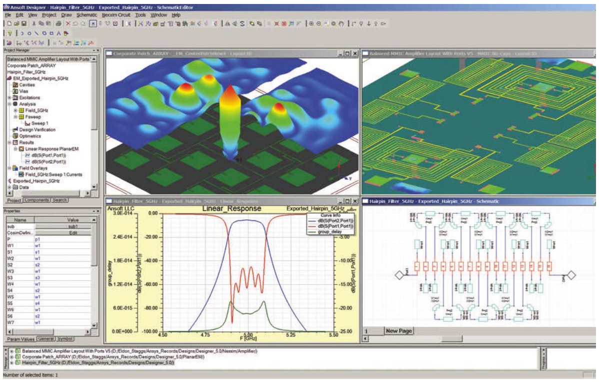


Simulation technology targets SI analysis and RF/microwave design

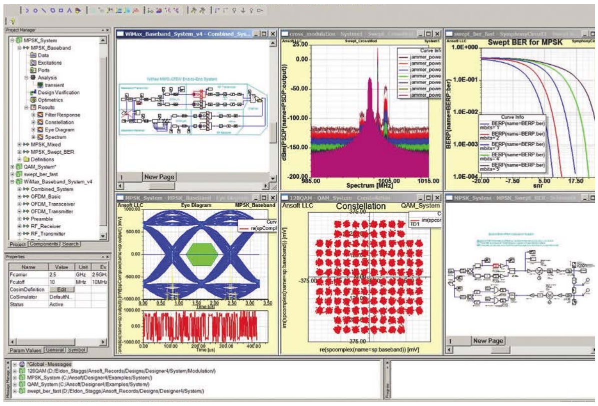
Ansys Inc has announced its Ansoft Designer 5.0 and Nexxim 5.0 engineering-simulation platform and integrated technology suite, which supports Ansys' trademarked simulation-driven product development. The new versions add features that compress electronic design and analysis. For example, links with Ansys DesignXplorer software enable experiments, sensitivity studies, and six-sigma design. In addition, a distributed-solve HPC (high-performance-computing) capability allows engineers to analyze process variations within a full SI (signal-integrity) analysis across a network of computers. For RF and microwave design, Ansoft Designer 5.0 with Nexxim 5.0 features a new system-simulation engine that allows engineers to simulate entire wireless systems and link to accurate transistor and EM (electromagnetic) models.

The suite also offers new product packaging that customizes and streamlines Ansoft Designer and Nexxim simulation technology into application-specific software tools for engineers focusing on SI analysis or RF and microwave design. The new packages, DesignerSI and DesignerRF, integrate technology from Ansoft Designer and Nexxim into application-specific, easy-to-use engineering platforms that are straightforward to acquire.

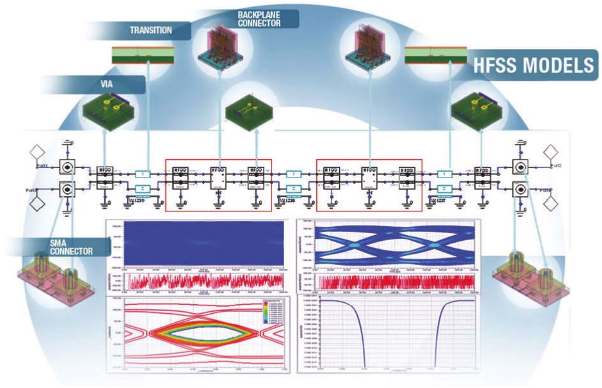
The DesignerSI package includes the Ansoft Designer schematic-capture and -layout graphical user interface, a 2-D quasistatic field solver, and the Nexxim circuit-simulation technology. DesignerRF includes the Ansoft Designer desktop, 3-D planar EM-field solver, RF-system-simulation tool, design-synthesis tools, and circuit simulation. Both packages include a design-management front end for Ansoft's HFSS (high-frequency simulator system), Q3D (quasi-three-dimensional) Extractor, and SIwave software.



The DesignerRF PlanarEM package includes 3-D planar electromagnetics with linear circuit-simulation capabilities.



The DesignerRF suite allows detailed component modeling or end-to-end system modeling of advanced communications systems.



You can perform high-speed serial channel simulation in DesignerSI using dynamic links to HFSS software.

The DesignerSI product suite targets engineers designing high-speed electronic interfaces, including XAUI (10-Gbps attachment-unit interface), SATA (serial advanced-technology attachment), PCIe (Peripheral Component Interconnect Express), HDMI (high-definition-multimedia interface), DDR, DDR2, and DDR3. Engineers using DesignerSI can leverage its optimization algorithms and design-of-experiments, tuning, and postprocessing capabilities for key SI metrics, such as TDR (time-domain reflectometry), BER (bit-error rate), timing analysis, and eye diagrams. All SI analyses can dynamically link to rigorous EM extraction. New SI-analysis features include IBIS-AMI (input/output-buffer-information-specification-algorithmic-modeling-interface) simulation, which fully supports the latest IBIS standard, enabling fast behavioral modeling of electronic systems with silicon vendor-supplied driver and receiver models, and QuickEye and VerifEye enhancements, which support separate rise/fall step responses, step-response parallel processing, improved BER noise floor, and enhanced jitter algorithms.

The DesignerRF product suite's new enhancements include a system simulator with baseband and envelope simulation of advanced communication systems, a filter-synthesis tool that generates ideal and physical filters for circuit and EM tools, and library expansion. For more on these products, go to www.edn.com/article/CA6709501.

—by Rick Nelson

▷**Ansys**, www.ansys.com.

Wireless-networking development kit supports real-world use

The eZ430-Chronos development kit delivers a programmable development environment for the CC430 microcontroller in a sports watch.

Texas Instruments' new eZ430-Chronos development kit delivers a programmable development environment for the CC430 microcontroller that resides within a wearable-sports-watch form factor. The development kit is available now for $49 and includes a CC430F6137 microcontroller that integrates two-way RF support, through the 5CC1101 RF transceiver, in the 433-, 868-, or 915-MHz frequency bands. The kit includes TI's SimpliciTI and BM Innovations' (www.bm-innovations.com) Blue Robin RF stacks to support out-of-box operation.

The kit integrates a three-axis accelerometer, an altimeter, sensors for temperature and battery voltage, and a 96-segment LCD that the CC430 drives directly. On-chip peripherals include a 100-nA comparator; an eight-channel, 200k-sample/sec, 12-bit ADC; an LCD controller; and a 128-bit AES (Advanced Encryption Standard) security encryption/decryption coprocessor. The 27-MHz CC430 can store in internal memory as much as 11 hours of data, such as from the companion BM-CS5 heart-rate monitor, which is available separately with a coupon.

To program the microcontroller, you disassemble the sports watch with an included screwdriver and attach it to an eZ430 programmer board that provides a USB (Universal Serial Bus) connection to your host computer. The USB-RF access point supports PC communication and includes production-ready source projects for motion-based mouse control, keyboard and presentation control, and time and calendar synchronization. The Chronos development kit includes projects with watch functions, such as time, date, alarm, and stopwatch; sensor data logging with wireless PC download; and motion-based mouse/PC-game control. User-generated applications are available at www.ti.com/chronoswiki.

—by Robert Cravotta

▷**Texas Instruments**, www.ti.com/chronos-pr.

VeriWave launches video-over-Wi-Fi test

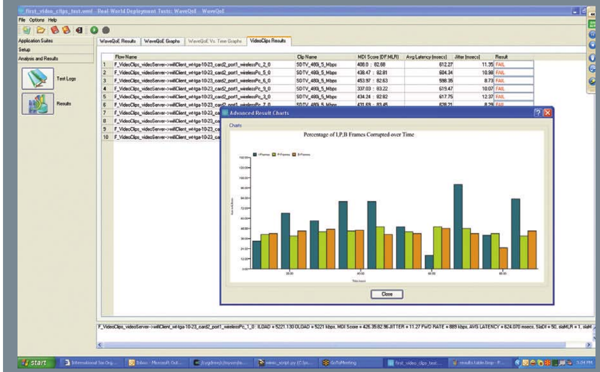
VeriWave has introduced its WaveVideo, which measures the quality of video streamed over Wi-Fi-based consumer services, video-security networks, and corporate videoconferencing services. The tool accelerates time to market for makers of Wi-Fi access points, video and media gateways, IP (Internet Protocol)-based video-surveillance cameras, and set-top boxes. Service providers and corporate IT departments can use the tool to help select vendors, optimize network design, and troubleshoot end-user problems. WaveVideo supports video ranging from low-quality VGA (video-graphics array) to high-quality HDTV (high-definition television).

The VeriWave tool can provide objective measures of quality using numerical values, or users can subjectively compare original video clips entering a system under test with the resulting video clip after it passes through that system. The tool also enables users to mix video traffic with other types of traffic, such as voice and data, to observe cross impact.

To help measure video quality on client devices, users can employ VeriWave's WaveAgent, a software utility taking up less than 200 kbytes, which you can load onto a client device to measure quality of experience from the end user's point of view. WaveAgent works with any client device–laptops, PDAs (personal digital assistants), and phones–connected to a wired or wireless network, including Ethernet and SONET (synchronous optical network), as well as Wi-Fi, GSM (global system for mobile communication), 3G (third generation), LTE (long-term evolution), and WiMax.

Prices for the WaveVideo application start at $7500 per licensed VeriWave test port. For more on these products, go to www.edn.com/091215pa.–by Rick Nelson

▶**VeriWave, www.veriwave.com.**



	Flow Name	Clip Name	MDI Score (DF:MLR)	Avg Latency (msecs)	Jitter (msecs)	Result
1	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_2_0	SDTV_480i_5_Mbps	408.0 : 82.68	612.27	11.35	FAIL
2	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_5_0	SDTV_480i_5_Mbps	438.47 : 82.81	604.34	10.98	FAIL
3	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_6_0	SDTV_480i_5_Mbps	453.97 : 82.63	598.35	8.73	FAIL
4	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_9_0	SDTV_480i_5_Mbps	337.03 : 83.22	619.47	10.07	FAIL
5	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_3_0	SDTV_480i_5_Mbps	434.24 : 82.82	617.75	12.37	FAIL
6	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_7_0	SDTV_480i_5_Mbps	431.69 : 83.45	628.21	8.29	FAIL
7	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_ca					
8	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_ca					
9	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_ca					
10	F_VideoClips_videoServer->wifiClient_wt4ga-10-23_ca					

F_VideoClips_videoServer->wifiClient_wt4ga-10-23_card2_port1_wirelessPc_1_0 : ILOAD = 5221.130 OLOAD = 5221 kbps, MDI Score = 426.35:82.96 JITTER = 11.27 FWD RATE = 889 kbps, AVG LATENCY = 624.070 msecs, SlaDf = 50, slaMLR = 1, slaM

The WaveVideo tool reports the percentage of I (intracoded), P (predicted), and B (bidirectionally predicted) frames that have become corrupt over time.

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Bring on the Converter Noise! – Part 2

Q. How does resistor noise compare to A/D converter's noise?

A. In the first installment Noise Figure (NF) considerations were discussed. Remember, think noise spectral density (NSD), here's why.

The A/D converter's total NSD performance is really a number of parameters like thermal noise, jitter, and quantization noise, ie — signal-to-noise ratio (SNR) over a specified bandwidth (BW). SNR reported in a converter datasheet, can give the designer a realistic expectation when trying to understand the converter's lowest resolvable "step" in the signal being sampled. This step, is also called a least significant bit or LSB. Given an N-bit converter and input fullscale value SNR and LSB size can be determined. Where, SNR = 20*log(Vsignal-rms / Vnoise-rms) and LSB = (Vrms Fullscale/(2^N)).

By re-arranging this equation, one can determine the converter's noise or Vnoise-rms = Vsignal-rms*10^-SNR/20. So, for a typical 16-bit, 80MSPS A/D converter with an SNR of 80dB that has a 2Vpp input full-scale will have a Vnoise-rms = 70.7uVrms or LSB size of 10.8uVrms.

Now let's look at resistor noise. Resistor noise is defined as Vresn = sqrt(4*k*T*BW*Resistance), therefore a 1kohm resistor adds about 4nV of noise in a 1 Hertz BW. Where T is temperature in Kelvin (room temperature = 290K), BW is bandwidth and k is Boltzmann's constant (1.38x10E-23 Watt/second/Kelvin). With respect to the converter resistor noise doesn't seem to be much to worry about. Don't be fooled.

Now let's continue to discuss driving down NF in order to increase sensitivity. This can be achieved by adding gain and resistance on the converter's frontend design. In the case of a passive frontend a decrease in the input full-scale by a factor of 2, means the NF goes down by 6dB. Yeah! However, consider the uncorrelated resistor noise as well.

The gain of 2 in the signal chain really makes a 50ohm resistor look like 14.4uVrms and the 200ohm termination resistor noise on the opposite side will add another 14.4uVrms. These two uncorrelated noise sources root sum square (RSS) together bringing the total noise to 20.3uVrms. That's 2 LSBs!

The point here is converter noise is >> bigger in terms of resistor noise even with some gain applied. However, as higher value resistors and gain are applied throughout the signal chain the total noise will easily start to erode SNR away (LSB = 1bit = 6dB). Be wary about employing gain in the signal chain, the factors add up fast.

To Learn More About
Noise Spectral Density (NSD)
http://designnews.hotims.com/23129-101

Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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Roy Vallee: Innovation must go on

Roy Vallee, a 37-year distribution-industry veteran and chairman and chief executive officer of Avnet Inc (www.avnet.com), discusses the year that was and the year to come, where opportunities are, and how innovation continued despite a turbulent 2009. A shortened version of that conversation with *EDN* follows. For the complete interview, go to www.edn.com/091215pb.

Analysts are suggesting that 2009 will see an 11 to 13% revenue decline versus estimates they made in the first quarter that called for a nearly 25% decline. What made this year less painful than it could have been for the electronics industry?

A The supply chain has reacted more dramatically to this economic slowdown than I have seen in my entire career in this industry. … By the time the industry saw a drop in demand, there was a very accelerated and aggressive movement to reduce inventories and cut back supply chains. In the early part of the year, the picture looked bleak. As the year has played out, companies have gotten their inventories in line with where they would like them to be, even with end demand being below where it was a year ago. As a result, they resumed purchasing. So the overreaction or initial aggressive reaction was not sustained for more than a couple of quarters. … Going into this [period], the industry was in pretty good shape from an inventory and a capacity perspective. As a result, we had to deal with the demand drop, but [the drop was different from that in] 2001. When we went into this slowdown, we didn't have massive amounts of excess inventory and capacity.

What did distributors do to help keep the inventory situation under control through 2008 and 2009?

A Distributors had been doing a good job before the slowdown at getting inventories in line or at appropriate levels. Distributors then reacted quickly to the slowdown in demand and actually got their inventories corrected in … a record time frame. The good news is that [reaction] helps reduce the duration of the correction. The bad news is that … while we were cutting back those orders with suppliers, suppliers were perhaps not so happy with us and disappointed with their actual incoming orders. But distributors did an excellent job of managing working capital before and during the slowdown.

Was fulfillment or demand creation/design chain more important in 2009? How about in 2010?

A What's more important: the heart or the brain? I don't think I can make this call. It depends on who you are talking to and at what point in time. The simple reality is that both of these requirements are absolutely vital to the electronics supply chain. It can't function without either one of them.

Do you think the layoffs in 2009 hampered the industry's ability to innovate and design?

A There had to be some negative impact … just associated with all of the distraction that went on. But I do want to say that most of the companies I know were focused on protecting their R&D resources and projects. A lot of the cutbacks were done in other areas. I'm not saying 100%, but I think innovation was protected and therefore negatively impacted less than other areas. … Innovation must go on.

What do you see for 2010?

A I think the industry is going to enter the year in pretty healthy shape; inventories and capacities will be in reasonably good shape. On top of that, end demand should improve. I'm not expecting an end-demand V curve, but I am expecting end demand to gradually improve, partly due to what normally happens when economic cycles hit a trough—and this one seems to have done so—and partly due to the still-substantial government stimuli that are happening and [are happening] in a way that will contribute to demand in 2010. It's going to be a much better year than 2009.

Are you particularly hopeful about any segments or regions for next year?

A From a geographic perspective, the first answer out of everyone's mouth is China. It is doing a good job with its stimulus package and driving indigenous demand. In end markets, [I'm hopeful about] medical, government, and some digital consumer markets, especially digital consumer for mass markets. More from a technology perspective, I would put solid-state lighting in a growth category, and wireless everything continues to expand. The other one that really seems to be having some impact is "green" technology. I think all of those areas are going to grow faster than the averages.

Do you think that the electronics industry is leading the United States' recovery?

A I do. The data supports the statement. The recovery in our business seems to be preceding the recovery in the macro economy and what's going on in the job market. Electronics technology allows for higher levels of productivity in business environments and improves the quality of people's lives. You can look at that from medical and health applications to good old-fashioned entertainment. Technology brings great value to the market in productivity and the quality of life.

—interview conducted and edited by Suzanne Deffree

BY PATRICK DORSEY

Spartan-6 FPGAs — The Crystal Clear Advantage in Flat Panel TVs

In the age of the flat panel display, top TV manufacturers have to be extremely innovative. They not only have to figure out what advanced feature set they'll include in their next line of TVs, they must differentiate their TVs from a growing number of competitors, then get those TVs to market quickly. The most innovative OEMs have figured out that the secret to staying on top and keeping their edge in the TV market is to use low-cost Xilinx® Spartan® FPGAs instead of ASSPs. In January, Xilinx in partnership with distributor Tokyo Electron Device Ltd. (TED) will make the Spartan FPGA advantage even more clear with the release of its Spartan-6 FPGA Consumer Video Kit.

A few years ago, OEMs dealt with these design and market challenges by using one ASSP-based chip set across multiple product lines. By creating various software features that leverage these chips' internal processors, they could quickly, though not too resoundingly, distinguish one TV's feature set from the others in their product line. Unfortunately, a slew of competitors followed suit and began using the same ASSP chip sets. This limited differentiation, forced the big OEMs to drop price points, which significantly deteriorated profit margins.

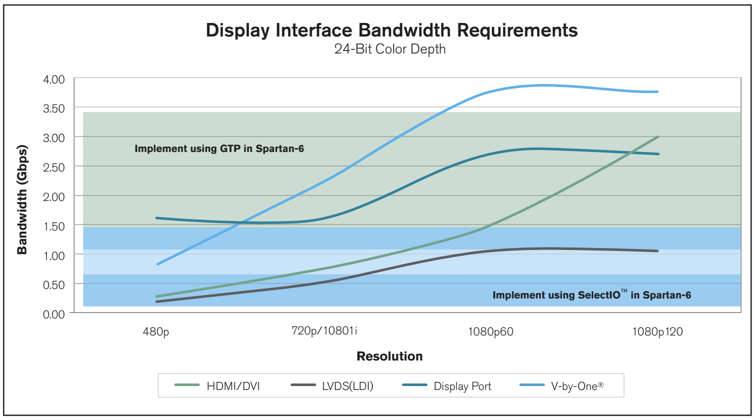
By switching to Spartan FPGAs, OEMs can quickly enhance and optimize the full hardware functionality (as well as software and algorithms) of each product and integrate the functions of multiple chips into a single FPGA—eliminating the restrictions of an ASSP-based solution that only allows for limited modifications. This transition from a multichip ASSP-based system to a single-chip FPGA-based system saves power, space, cooling and improves overall system performance, while reducing overall bill of materials cost, and, above all, enabling end-product differentiation.

What's more, the Spartan series' proven reliability and reprogrammability has helped OEMs drastically reduce defect rates and increase margins as well as consumer satisfaction, garnering their Spartan FPGA-based flat panel displays critical acclaim from editors and customers alike.

To build on this success in the consumer TV market and help OEMs and their suppliers leverage the integrated 3.125Gbps serial transceivers and other advanced features of Xilinx's new Spartan-6 family, in January Xilinx will announce the availability of the Spartan-6 FPGA Consumer Video Kit.

This easy-to-use and expandable kit will include a baseboard along with several FMC daughter cards, integrating soft IP logic blocks from Xilinx and its partner TED to support emerging and de facto high-speed display interfaces, including DisplayPort, V-by-One, high-speed LVDS and HDMI. The kit will streamline customer algorithm development on Spartan-6 based systems and give designers a jump on bringing differentiated products to the market quickly.

To learn more about the Spartan FPGA advantage, visit the Consumer Page at www.xilinx.com/consumer.



With integrated 3.125Gbps serial transceivers, the Spartan-6 family is ideally suited to support increasing line rate and bandwidth requirements of emerging TV standards.

About the Author: Patrick Dorsey is the Sr. Director Product Management at Xilinx Inc. (San Jose, Calif.). Contact him at more_info@xilinx.com

BY BONNIE BAKER

Common-mode range can bite hard

My last column provided a glimpse inside the CMR (common-mode rejection) of a three-op-amp INA (instrumentation amplifier) and revealed the main contributors to total CMR error (see "Understanding CMR and instrumentation amplifiers," *EDN*, Nov 26, 2009, pg 14, www.edn.com/article/CA6707779). This story goes deeper, however, if you look at the common-mode range of the same device. Of all the performance characteristics of an INA, the most misunderstood is the common-mode-range requirement. So how do designers calculate the INA's common-mode range? Consider the exposure to an input/gain-overload condition on the INA as a possibility.

Three basic kinds of nodes in the INA can cause input/gain-overload problems (**Figure 1**). Pay attention to the voltage levels of the INA's V_{IN+} and V_{IN-} input pins, the V_{OA1} and V_{OA2} output levels of A_1 and A_2, and the V_{OUT} output-swing capability of A_3. As you work with these concepts, you may notice that an input signal into an INA can produce an incorrect output signal that is nevertheless within the device's normal output range.

The applied input voltages to the INA are equivalent to the common-mode input voltage plus or minus the differential input signal. The input stages of A_1 and A_2 limit the range of these two input voltages. The maximum and minimum input-voltage limits vary from device to device.

The input voltages at V_{IN+} and V_{IN-} and the gain of A_1 and A_2 cause the internal output voltages to increase or decrease. Note that the A_1 and A_2 stages do not gain the input common-mode voltage, V_{CM}. An input/gain-overload condition can occur if A_1's output voltage, A_2's output voltage, or both violate the internal output-swing restrictions. This condition is impossible to directly measure. You must be aware of the limitations of V_{OA1} and V_{OA2} and then calculate whether your design is at risk using the **equations** in **Figure 1**.

An example of this type of input/gain-overload condition occurs when the in-range voltages on the INA's inputs drive A_1, A_2, or both to their positive or negative output-swing limit. In this condition, A_3 measures an erroneous difference voltage. This erroneous voltage plus the voltage reference to the INA is incorrect and may be inside the output range of A_3.

The final place to look for an input/gain-overload condition is at the output, V_{OUT}, of the INA. The A_3 output restrictions are similar to those of any other amplifier. For instance, in a single-supply environment, the output swing never spans all the way to the rails.

The common-mode behavior of the three-op-amp INA may surprise you if you ignore the nuances of the internal A_1 and A_2 output stages. All of the internal amplifier's output voltages relate to the linear common-mode input range of the complete INA. Most product data sheets provide illustrations of the effects of input/gain-overload conditions. You can now use those graphs to your advantage.**EDN**

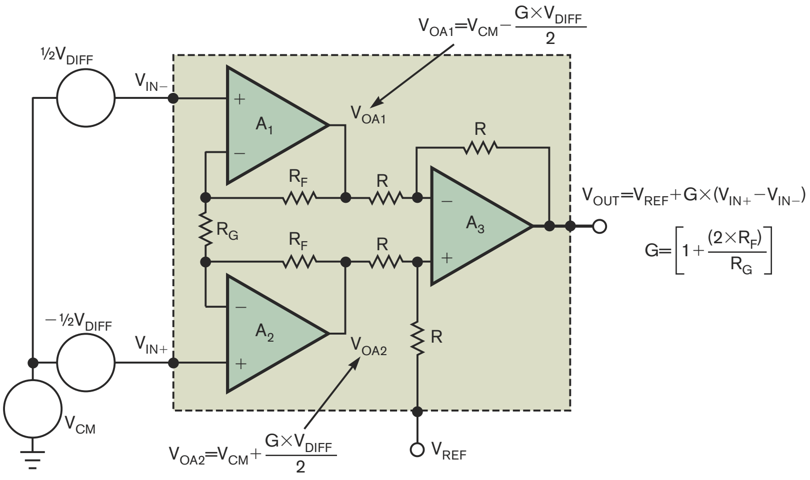
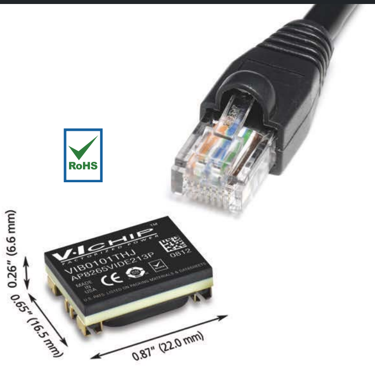


Figure 1 Three basic kinds of nodes in an instrumentation amplifier can cause input/gain-overload problems.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

⊞ www.edn.com/bakersbest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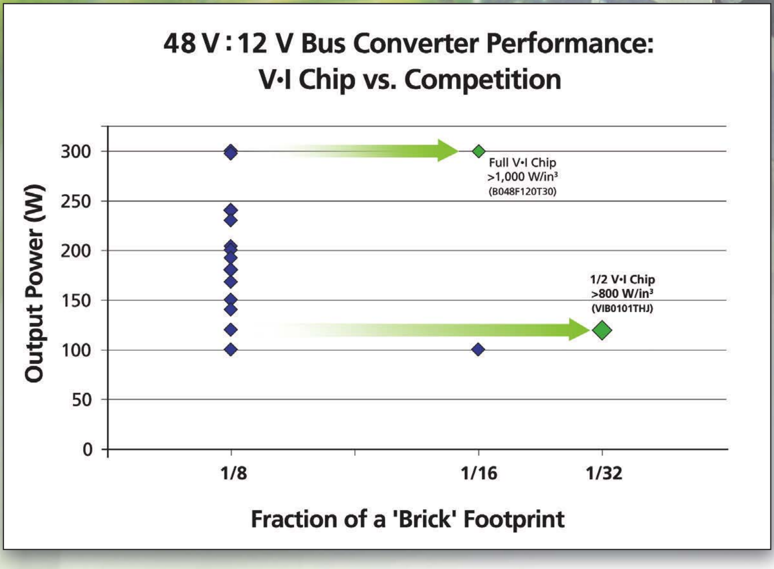

Output Power (W)
300
250
200
150
100
50
0
1/8
1/16
1/32
Fraction of a 'Brick' Footprint
Full V·I Chip
>1,000 W/in^3
(B048F120T30)
1/2 V·I Chip
>800 W/in^3
(VIB0101THJ)

RON WILSON • EXECUTIVE EDITOR

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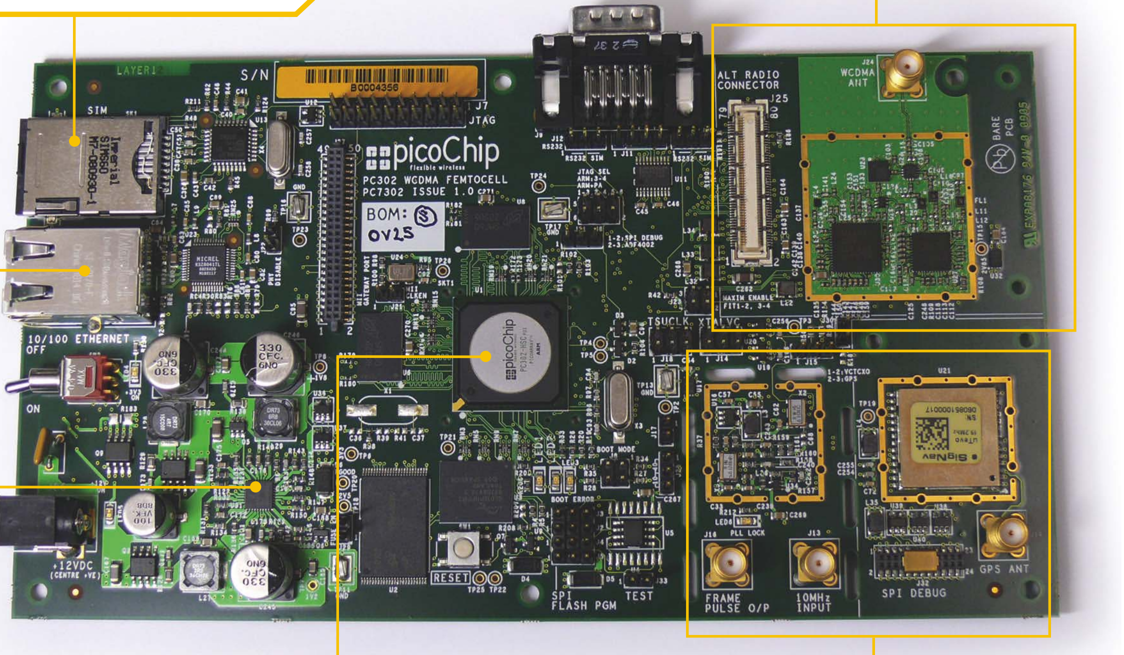
Inside a cellular femtocell

Cellular-service providers are trying to shore up their service by selling femtocells to customers. These little boxes have to sell for at most a few hundred dollars and be both user-installed and self-configuring. And they must provide most of the functions of a full cellular base station. On power-up, the femtocell configures itself to take advantage of the most available radio frequencies at its current location, establishes an IPsec (Internet Protocol-security) connection through the user's Wi-Fi or wired Ethernet back to the carrier's femtocell gateway, and checks itself into the carrier's wireless network.

To get all of these functions into this price range and into a form factor similar to that of a Wi-Fi hub, designers lean heavily on both a highly integrated, application-specific system chip and carefully optimized radio and power circuits. This evaluation-level reference design of an HSPA (high-speed-packet-access) femtocell from silicon vendor PicoChip illustrates the implementation and the care that will go into femtocell designs. Note that this unit is a lab development board, not an optimized product. As such, it has a lot of test points, debugging connectors, and so on. It also has some duplication—for example, several memory types.



Some carriers use the optional SIM (subscriber-identity-module) card for authentication and security.

The femtocell requires a variety of radios: an HSPA Node B transmitter and receiver for femtocell operation, an HSPA UE (user-equipment) receiver for hand-over and network-monitor functions, and a GSM (global-system-for-mobile) communications UE receiver for hand-over.

An Ethernet broadband connection routes traffic back onto the wired Internet.

The board requires a variety of power supplies at the lowest possible cost.

The low-cost, low-power, fully integrated PicoChip PC302 baseband SOC (system on chip) integrates a Node B modem; a controller, including an RNC (radio-network controller) and all associated functions; interference management; and peripherals.

Either an NTP (network-time protocol) from the left-hand module or an A-GPS (assisted-global-positioning-system) circuit from the right-hand module provides timing and synchronization for stationary indoor applications.

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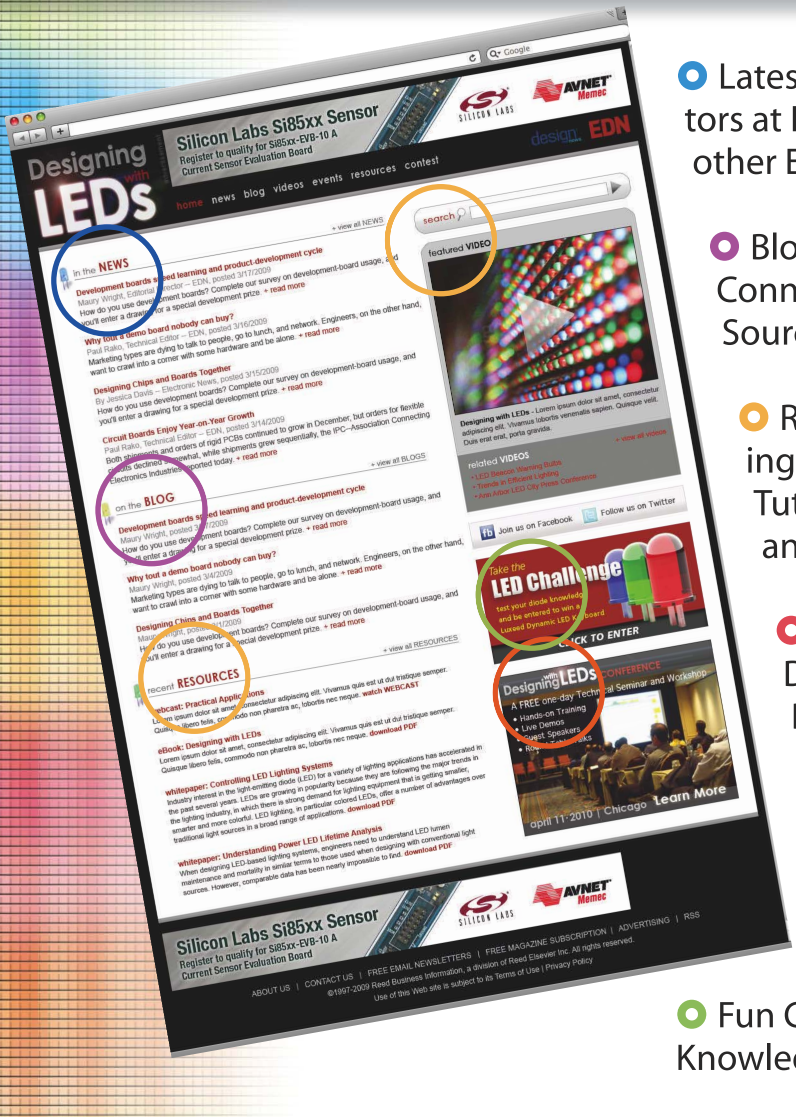

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MODEL-BASED DESIGN AND EARLY VERIFICATION AID DESIGNERS

MODELING AND SIMULATION AT LEVELS RANGING FROM CHIP TO SYSTEM CAN CATCH BUGS EARLY AND ENSURE QUICK TIME TO MARKET.

BY RICK NELSON • EDITOR-IN-CHIEF

Engineers can save themselves a lot of grief if they carefully evaluate their designs in software before committing to silicon or sheet metal. Model-based-design and early-verification tools are helping designers, whether they are developing ICs or airframes, find inevitable mistakes early and get to market on time. Model-based design can be of significant value in helping isolate domain experts, such as medical-device or aerospace engineers, from the need to understand low-level hardware and software details (**Reference 1**). However, they can also help catch errors at the specification stage that designers would not otherwise catch until the test stage, saving time and money. The available modeling and prototyping tools span the gamut of applications, from mechatronics systems to RTL (register-transfer-level)-IP (intellectual-property)-based SOCs (systems on chips).

Not surprisingly, the automotive industry is aggressively using model-based design and simulation as it grapples with new technologies, such as hybrid-electric and fuel-cell vehicles. A recent article describes automotive-R&D activities as comparable to those of the telecommunications industry when it overcame power and chip-size challenges to support the evolution of cell phones into multimedia devices (**Reference 2**). The article touts simulation as a way to meet the challenges, citing Mentor Graphics' SystemVision, for example, as a simulator that can help engineers manage mechanics, electronics, software, and controls all in one system.

Model-based design and rapid prototyping can be particularly valuable in proof-of-concept work or in ensuring that a specification meets customer requirements. Alliance Spacesystems, for example, uses the concept in its development of robotic arms for applications including the Mars Spirit and Opportunity rovers (**Reference 3**). Sean Dougherty, mechatronics-group supervisor at the company, describes a Hubble-space-telescope application in which replacement of a malfunctioning instrument would require the removal of 100 fas-

AT A GLANCE

- The automotive industry is using model-based design and simulation as it grapples with new technologies, such as hybrid-electric and fuel-cell vehicles.
- Simulations often do not connect to requirements, a problem that you can address through the definition of requirements-based test.
- For algorithm-intensive applications, engineers are spending 50% or more of their time writing verification code.
- In the software-differentiated hardware era, software development costs will represent more than 70% of total development costs as process geometries shrink to 22 nm.
- It has become as difficult to handwrite cycle-accurate models as it is to write the underlying RTL (register-transfer-level) code.

teners. NASA (National Aeronautics and Space Administration), he says, was not sure the feat was possible. Using hardware and software from National Instruments, however, Alliance Spacesystems within three months prototyped a functioning robot with X-, Y-, and Z-axis motion, complete with a vision system to recognize the fasteners.

A more down-to-earth application for Alliance Spacesystems involves automobile-mounted camera booms that the movie industry uses to film car chases. Although aerospace and similar programs tend to have long leadtimes with thoroughly reviewed specifications and requirements documents, filmmakers are more likely to require frequent iterations to obtain what they want. Hardware and software, such as National Instruments' LabView and CompactRIO platform, says Dougherty, enable him to adapt to customers' evolving needs, rapidly developing new versions.

Brett Murphy, manager of technical marketing at The MathWorks, lays out

TOMORROW'S ENGINEERS LEARN MODEL-BASED DESIGN

The engineers of tomorrow are getting a taste of model-based design and simulation through programs such as EcoCar: The Next Challenge, which has the support of the US Department of Energy, General Motors, The MathWorks, Freescale Semiconductor, National Instruments, and other sponsors that are lending time, money, and products to the university-level competition. The EcoCar program began in the fall of 2008 when students from 17 universities in the United States and Canada began a three-year effort to design and re-engineer a 2009 Saturn Vue to be more efficient and reduce emissions (references A and B).

Speaking at a kickoff meeting for the second year of the program, which took place at The MathWorks headquarters in Natick, MA, Mike Wahlstrom, a control and simulation engineer at the Center for Transportation Research at the Energy Systems Division of Argonne National Laboratory, said that EcoCar is the latest effort in the 20-year history of advanced-vehicle-technology competitions. Wahlstrom began his career with the competitions as a student and now assists in organizing the program, which Argonne manages for the Department of Energy.

For the first year of the program, teams worked only on model-based design and simulation. Vehicles began arriving this fall, and teams will spend the second year building a "mule vehicle," a term the teams borrowed from GM's global-development program. A mule vehicle will be 60 to 65% ready to go. During the final year, teams will refine their vehicles to bring them nearer a production state.

Chad Conway, a sophomore at Rose-Hulman Institute of Technology, joined the team last winter and has been using MathWorks and National Instruments tools to investigate vehicle design. Zachery Chambers, an associate professor of mechanical engineering at the school, says that the team is working on a parallel pretransmission/post-transmission electric hybrid. The vehicle will have a downsized 1.3l diesel engine. Between it and a stock four-speed automatic transmission, the team will insert an electric machine to provide additional capability to the engine to offset its downsizing. In addition, the team will place another electric machine on the rear axle to provide for regenerative braking and additional acceleration.

As for the importance of model-based design and simulation, Chambers says, the biggest mistake teams can make is to take a wrench to their vehicles too early. "When they have an operational vehicle, it really behooves teams to use their CAN [controller-area-network]-analysis tools to tap into the vehicle network to make sure they can communicate with all the modules inside the vehicle and go out and collect some baseline data." Chambers advises the teams to figure out their testing procedure now while they have something that works before they try to "figure out a testing procedure with something that may or may not work all that well."

See the online version of this article for more on EcoCar and other applications for model-based design and simulation.

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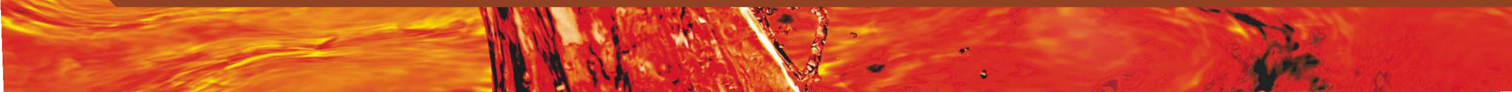
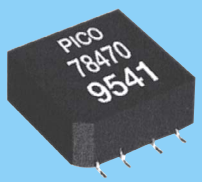
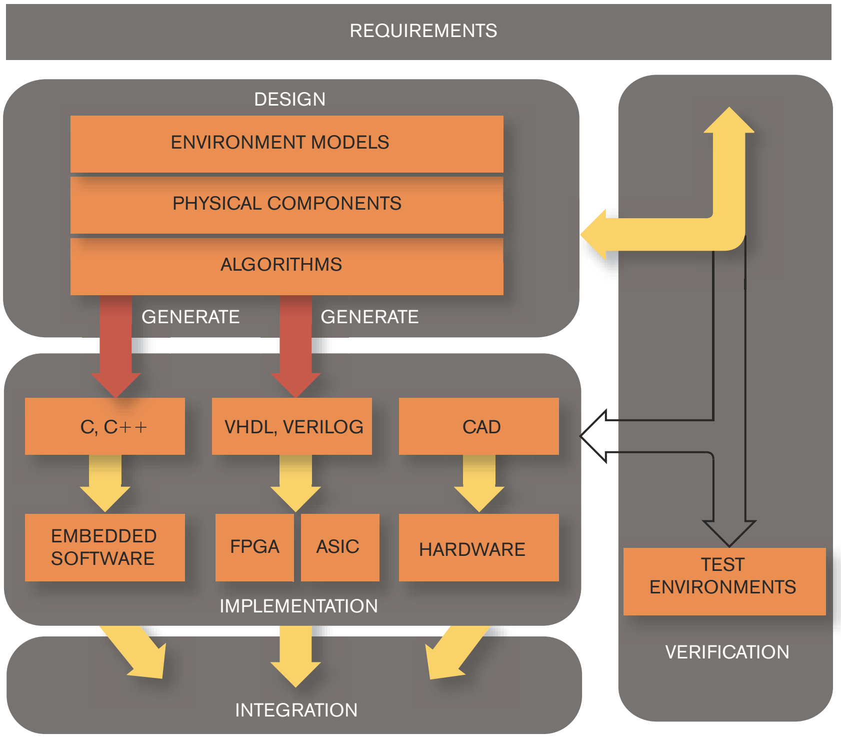




the case for early verification. He says that aerospace and automotive members of the company's customer-advisory boards cite verification and validation as top priorities. Errors most often emerge at a project's specification stage, and fewer errors manifest themselves at the subsequent design, implementation, and test stages. In contrast, engineers frequently don't detect the errors until the test stage. Murphy presents a multistage approach to catching and correcting errors earlier. This approach includes capturing requirements using executable specifications; using models as the system-level test benches for algorithms and components; simulating to explore design trade-offs, component interactions, and system-level metrics; and reusing the same test bench from virtual system integration through to the developed system. These techniques are applicable to adopters of model-based design; groups developing control systems; and engineers designing algorithm-intensive signal-processing, imaging, and communications systems.

ERRORS MOST OFTEN EMERGE AT THE SPECIFICATION STAGE; FEWER ERRORS MANIFEST THEMSELVES AT THE DESIGN, IMPLEMENTATION, AND TEST STAGES.

For adopters of model-based design, Murphy adds, simulations often do not connect to requirements, a problem that designers can address through the definition of requirements-based test in a process that enables the use of simulations to ensure designers find requirements errors early. Companies that have successfully employed the approach include Bell Helicopter. In addition, Murphy says, Hyundai has employed MathWorks and SimuQuest tools to model, simulate, prototype, and deploy an engine-control unit. The MathWorks is also involved

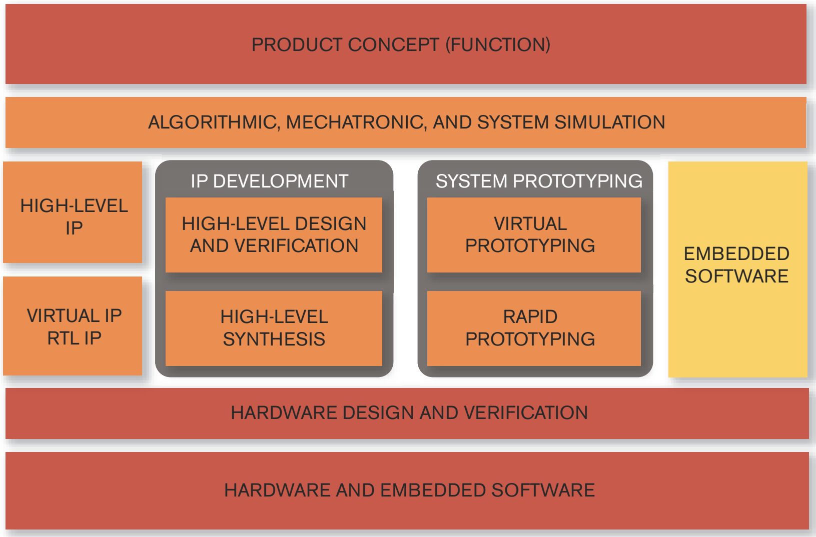


Problems can occur when simulations do not connect to requirements. One approach is to define requirement-based tests and employ simulations to ensure that you find requirements and design errors (courtesy The MathWorks).

in the EcoCar challenge for engineering students (see **sidebar** "Tomorrow's engineers learn model-based design").

Control-system designers, Murphy says, face challenges as system complexity grows. It then becomes important to test control algorithms through modeling and simulation and to leverage models through automatic code generation for a microcontroller, an FPGA, or a programmable-logic controller to support real-time testing. Murphy notes that Manroland has employed MathWorks tools to design and model a printing-press controller, run real-time simulations, and deploy a production system, reducing development time by a year.

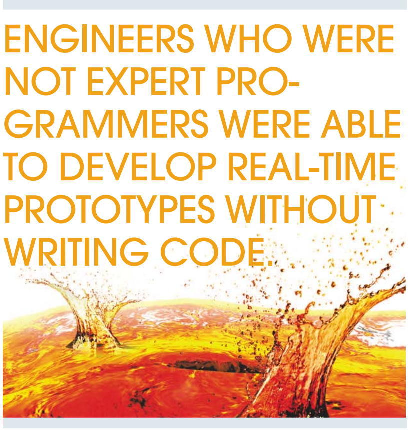
For algorithm-intensive signal processing in communications, electronics, semiconductor, imaging, medical, and aerospace applications, verification time and costs are escalating, with engineers spending 50% or more of their time writing verification code. To alleviate the problem, engineers can turn to multidomain system verification, integrating Matlab, C/C++, and HDL (hardware-description-language) IP into Simulink



System-level offerings from Synopsys span the gap from product concept to a hardware and embedded-software implementation: Saber, System Studio, and Innovator for algorithmic, mechatronic, and system simulation; the DesignWare, System Studio, and Synphony libraries of high-level IP; DesignWare cores for virtual IP and RTL IP; System Studio for high-level DSP design and verification; Synphony HLS (high-level synthesis); Innovator for virtual prototyping; Confirma for rapid prototyping; and core tools for hardware design and verification (courtesy Synopsys).

models. Designers can develop a golden reference model in Matlab, develop a test bench in Matlab or Simulink, and perform cosimulation with embedded IDEs (integrated development environments), HDL simulators, or analog simulators, leading to a DSP or an FPGA prototype without requiring low-level programming. Murphy adds that acoustical engineers from Philips, who were not expert programmers, were able to develop and test real-time prototypes for a surround-sound system without writing any low-level DSP code.

ENGINEERS WHO WERE NOT EXPERT PROGRAMMERS WERE ABLE TO DEVELOP REAL-TIME PROTOTYPES WITHOUT WRITING CODE.



SOFTWARE DIFFERENTIATION

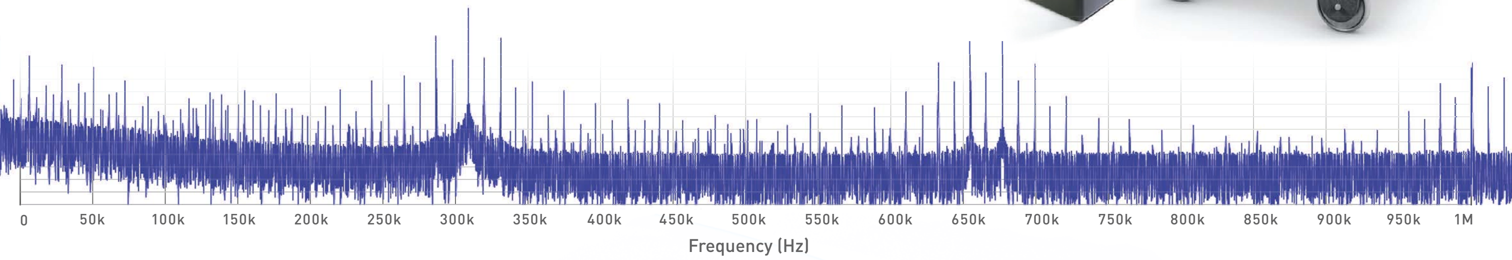
Frank Schirrmeister, director of product marketing for system-level solutions at Synopsys, sees the emergence of the software-differentiated-hardware era as a key challenge, with software-development costs beginning to represent more than 70% of total development costs as process geometries shrink to 22 nm. Citing IBS Research and Consultancy, he says the software costs were less than 20% of total development costs at the 180-nm node. Synopsys' own research reflects the trend toward higher software costs. As a result, designers are using embedded processors within their designs to verify the hardware—for example, by running test benches.

Synopsys offers a variety of system-level tools, including Saber, System Studio, and Innovator for algorithmic, mechatronic, and system simulation; the DesignWare system-level library of high-level IP; DesignWare cores; System Studio for high-level DSP design and verification; Innovator for virtual prototyping of embedded software; Confirma for rapid prototyping; and core tools for hardware design and verification. One of the company's newest tools in this market is the Synphony high-level-synthesis tool, which debuted in October. It converts Matlab M scripting-language code to synthesizable datapath-RTL logic.

Synopsys' DSP-algorithm portfolio enhances verification productivity through HDL-import and SystemC-export capabilities and maximizes simulation performance. System Studio supports algorithm optimization and verification using an executable test bench. The DesignWare system-level library combines with Innovator to support early software development and enhance design quality through a SystemC-executable specification.

CYCLE-ACCURATE MODELING

Carbon Design Systems focuses on cycle-accurate IP modeling for virtual prototyping of SOCs, providing presilicon validation of hardware and software designs. The company offers a compiler that reads in RTL in VHDL (very-high-



speed hardware-description language) or Verilog and produces a model that you can link into almost any virtual platform, including Carbon SOC Designer, CoWare Platform Architect, and OSCI (Open SystemC Initiative) SystemC (**Reference 4**). Cycle-accurate models in a language such as C represent the RTL from which designers compile them and consequently are more suitable for SOC validation than are models you derive from behavioral descriptions, which may not match the RTL performance.

According to Bill Neifert, Carbon's vice president of business development, the company has recently been working with ARM and MIPS Technologies on cycle-accurate models for increasingly complex processors. "Continuing handwriting cycle-accurate models was becoming too onerous a task [for ARM] as the company developed more and more advanced processors," he says. "It turned out it was just as much work to write the cycle-accurate models as it was to write the RTL for the real design." As a result, ARM decided 18 months ago to stop handwriting models. "That's when we stepped in and said that model generation happens to be a problem that we've solved," says Neifert. Carbon then acquired ARM's SOC Designer tool, which handles model generation for ARM IP, generating 100%-accurate models for ARM RTL IP and integrating features such as debuggers and program loaders. MIPS faced similar challenges in handwriting cycle-accurate models. "Seeing what we are able to do with the ARM processors, MIPS decided to follow a similar path," Neifert adds. MIPS, however, chose to employ Carbon's technology to generate its own cycle-accurate models of IP, such as its M14K and M14Kc cores, for its customers.

IP providers such as ARM and MIPS aren't the only customers for Carbon's technology. Last month, Carbon announced that AppliedMicro, which addresses energy-conscious computing and communications applications, selected Carbon Model Studio to accelerate the deployment of SystemC-based virtual platforms for presilicon and postsilicon software development, performance analysis, and validation of SOC designs.**EDN**

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ANALOG FLOATING-GATE TECHNOLOGY COMES INTO ITS OWN

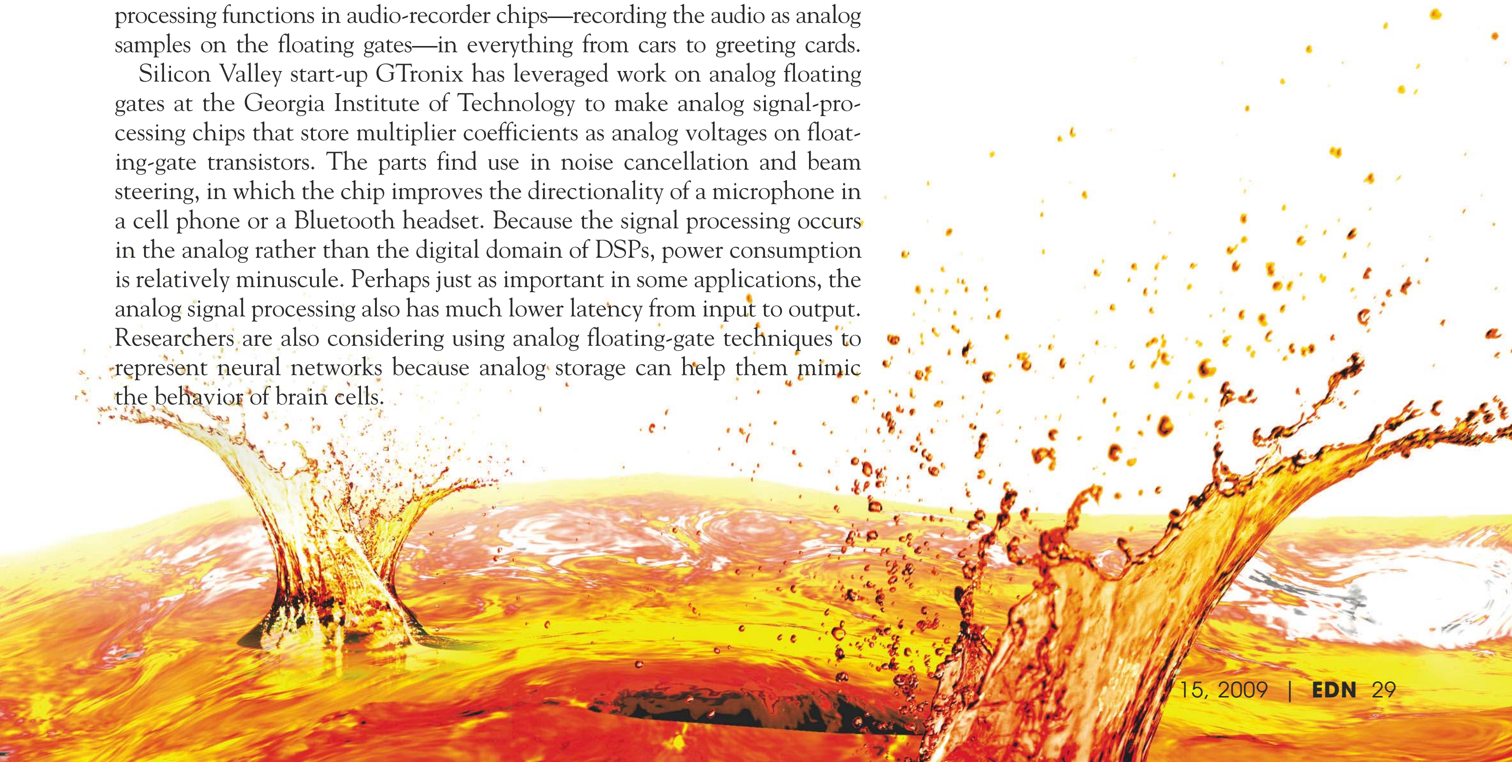
NO LONGER AN ANOMALY, ANALOG FLOATING-GATE TECHNOLOGY NOW FINDS USE IN EVERYTHING FROM CARS TO GREETING CARDS.

BY PAUL RAKO • TECHNICAL EDITOR

Just as its name implies, a floating-gate transistor's driving terminal is electrically isolated from the rest of the device—that is, floating—so there is no direct internal dc path from the input terminal to the other terminals. Semiconductor companies became aware of this technology more than 40 years ago when they examined "defective" ICs that had broken electrical connections to the gate terminal. Little did they then know that they could use digital versions of these floating-gate transistors to store information in memories.

Over the last 10 years, however floating-gate design has emerged as a technique not just for memories but also for many classes of ICs. For example, you can use the gate voltage to represent a trim level for internal circuit nodes. Voltage references can also store the output voltage on a floating gate, and you can use floating-gate analog circuits to implement advanced signal-processing functions in audio-recorder chips—recording the audio as analog samples on the floating gates—in everything from cars to greeting cards.

Silicon Valley start-up GTronix has leveraged work on analog floating gates at the Georgia Institute of Technology to make analog signal-processing chips that store multiplier coefficients as analog voltages on floating-gate transistors. The parts find use in noise cancellation and beam steering, in which the chip improves the directionality of a microphone in a cell phone or a Bluetooth headset. Because the signal processing occurs in the analog rather than the digital domain of DSPs, power consumption is relatively minuscule. Perhaps just as important in some applications, the analog signal processing also has much lower latency from input to output. Researchers are also considering using analog floating-gate techniques to represent neural networks because analog storage can help them mimic the behavior of brain cells.



Digital floating-gate technology—and its analog counterpart—has had a lengthy evolution, which began in the late 1960s at Bell Labs, when researchers Dawon Kahng and Simon Sze evaluated the uses of charge storage on insulated gates. They hoped to use this storage as a replacement for ferrite-core magnetic memories (**Reference 1**). This research was an outgrowth of Kahng's 1960 patent on FETs (field-effect transistors). In 1968, Horst Wegener, a researcher at Sperry Rand, received a patent on a FET memory element using charge stored on dielectrics, much as an electret microphone stores charge in wax.

By 1971, Intel's Dov Frohman had filed a patent for a floating-gate device that designers programmed using an electron tunneling through oxide. This technology forms the basis of most current floating-gate memory. In 1972, Frohman received a patent for EPROM (erasable programmable read-only memory), which requires you to irradiate the die with UV (ultraviolet) light to erase the memory. By 1978, George Perlegos, also at Intel, had developed a floating-gate EEPROM (electrically erasable PROM, **figures 1** and **2**). In 1980, Fujio Masuoka at Toshiba developed flash memory, the ubiquitous storage medium that now finds use in everything from USB (Universal Serial Bus) sticks to MP3 players to digital cameras and solid-state disk drives. Flash memory does not allow you to erase individual memory locations as EEPROM does but is far cheaper to manufacture, as prices for memory sticks demonstrate.

Analog techniques have also crept into the flash-memory arena. SLC (single-level-cell) solid-state flash drives work like traditional memory cells: You program the cell to either a one, which is full voltage, or a zero, representing no voltage. MLC (multilevel-cell) memory incorporates more analog elements. You program a cell to one of four levels, representing 2 bits of data, effectively doubling the memory capacity. Everything in the analog domain comes with trade-offs, however. For example, with MLC drives, you gain capacity at the expense of a worse BER (bit-error rate) and a reduced lifetime because you cannot overwrite MLC devices as many times as you can SLC devices. MLC devices also require error-correction circuitry to reduce the BER.

AT A GLANCE

- Analog floating-gate storage builds on EEPROM (electrically erasable-programmable-read-only-memory) and flash-memory technology.
- Applications for analog floating gates include analog recording, voltage references, and analog signal processing.
- Analog storage and signal processing yield significant power savings.
- Analog processing also offers low latencies.
- Producing successful ICs requires good understanding of design, process, and manufacturing.
- The potential uses for analog storage and processing are limitless.

ANALOG EVOLUTION

In 1988, Richard T Simko of ISD (Information Storage Devices, now Nuvoton), built on the digital floating-gate patents he obtained in 1979 while at Xicor with a patent for high-density-IC analog signal recording and playback (**Figure 3**). This patent was the basis for Nuvoton's ChipCorder, an analog IC that records and plays back audio using floating-gate storage techniques. As Simko states in the patent, the device can electronically store analog information with reasonable precision but with substantially less complexity and memory capacity than digital techniques require. With the system, small errors in recording the signal information do not damage the reproduction quality during playback.

Analog audio storage has many advantages over digital methods. For example, a digital-memory audio system might record 8000 8-bit samples/sec, whereas an analog memory cell could store that same sample in one cell, an eight-to-one advantage. As Geoff Jackson, chief technology officer at Nuvoton, notes, analog floating-gate technology with large memory cells and 8-bit samples can achieve fidelity equivalent to that of 10- or 12-bit samples. Farid Noory, senior technical-marketing manager at the company, notes that the parts can sample analog data at a 4- to 16-kHz sampling rate.

Programming a floating-gate memory cell to a desired analog voltage is not trivial (**Figure 4**). It involves the layout geometries, the thickness of the insulating oxide, and the field-strength profiles of each cell, so you cannot be sure that every cell you expose to an identical programming pulse will program to the same analog voltage. One of Simko's fundamental contributions provides for a series of pulses to the floating gate. The chip measures the resultant analog programmed voltage after each pulse, so that programming circuitry can stop the pulses when each cell reaches the proper voltage. As Simko notes in his 1988 patent, writing is an iterative, trial-and-error process because the analog input signal is only 1 to 2V, for example, and the voltage to charge a floating-gate memory cell may be 7 to 17V. Further, he notes, programming a cell may require as many as 400 pulses, but the chip can program a column of memory cells at once, with the iterative programming process occurring in parallel.

Today, Nuvoton calls its analog float-

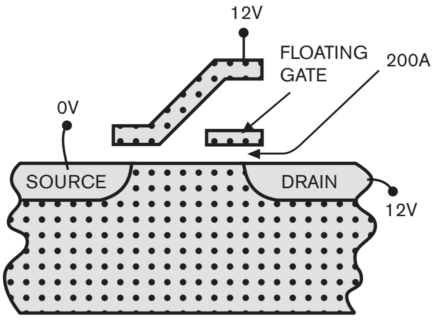


Figure 1 You program this floating-gate memory cell by putting 12V on the metallization over the floating gate. Electrons tunnel through the insulating oxide layer to program the gate.

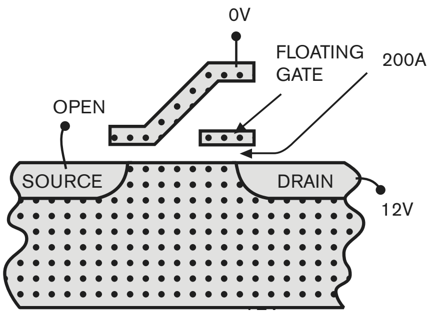


Figure 2 You erase this floating-gate memory cell by changing polarities to discharge the gate.

ing-gate parts MLS (multilevel-storage) devices, with which it implements a complete audio-recording and -playback SOC (system on chip, **Figure 5**). The ChipCorder IC includes a voltage regulator, a charge pump to make the programming voltage, a microphone preamplifier, memory, a PWM (pulse-width-modulated) power amplifier to run the speaker, the analog memory array, switch-debouncing circuits, and an SPI (serial peripheral interface) to a computer. The parts won an *EDN* Innovation Award in 1991, and Simko and his co-workers Trevor Blyth and Sakhawat Kahn were finalists for Innovators of the Year in *EDN*'s 1991 Innovation Awards (**Reference 2**).

The analog storage paradigm works well and is cost-effective for short recordings. For example, the ISD5216 chip uses analog floating gates to record and play back 16 minutes of audio. For longer recordings, Nuvoton offers chips such as the ISD151016, which uses digital storage, conventional flash memory, DACs, and ADCs, to record and play back 16 minutes of audio with better SNR (signal-to-noise ratio) than analog techniques can achieve. Deciding on an analog memory versus a digital one depends on your budget, taking into account the costs of flash versus those of an analog process. Analog processes tend to have larger features than those of a current flash-memory die with its 45-nm features.

DC IS ANALOG, TOO

As early as 1989, researchers had proposed the use of floating-gate analog FETs as a trimming element for ICs (**references 3** and **4**). Then-start-up Impinj planned to use floating-gate structures to hold analog trimming voltages. In 2003, the company tried to develop a floating-gate circuit using conventional high-density CMOS, instead of the CMOS process with larger features and more process layers that EEPROM cells use. At the time, the company's Web site touted its mission as "developing floating-gate transistors that are analog memory devices but [that] retain all the attributes of conventional CMOS transistors." The practical aspects of this approach proved so difficult that

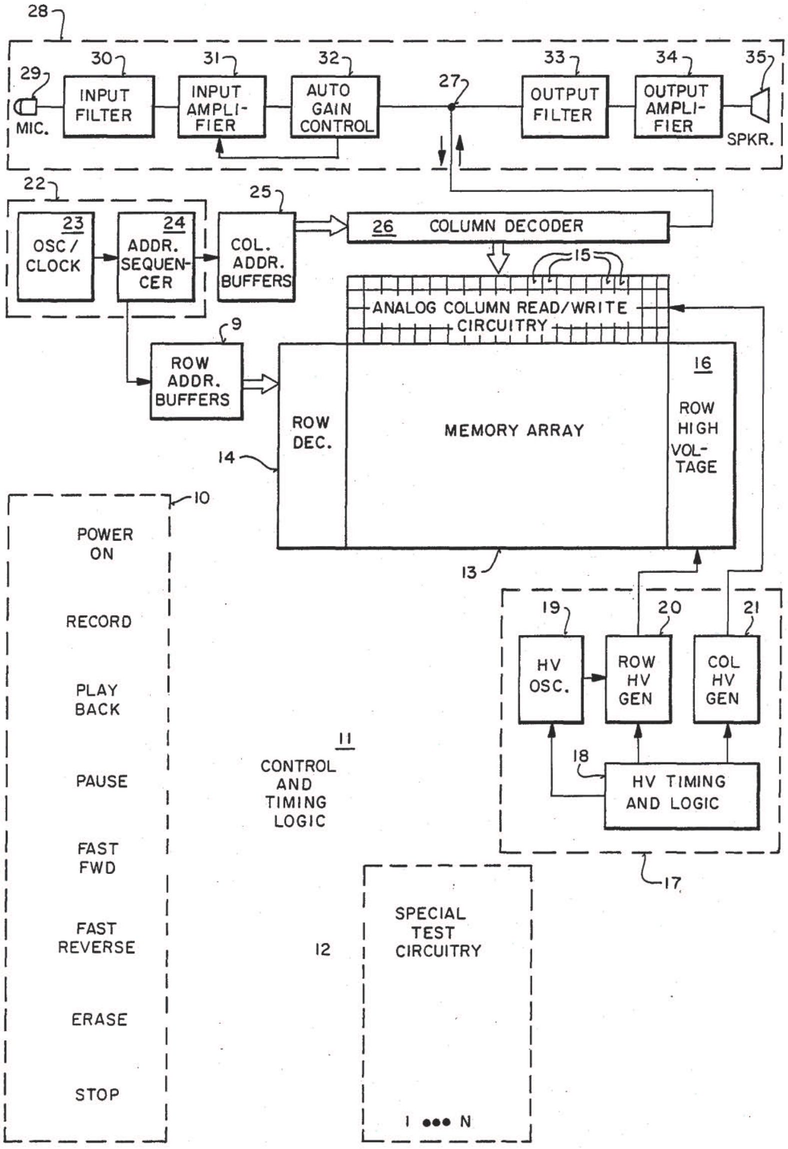


Figure 3 The 1989 patent on floating-gate analog audio storage describes the architecture of the chips.

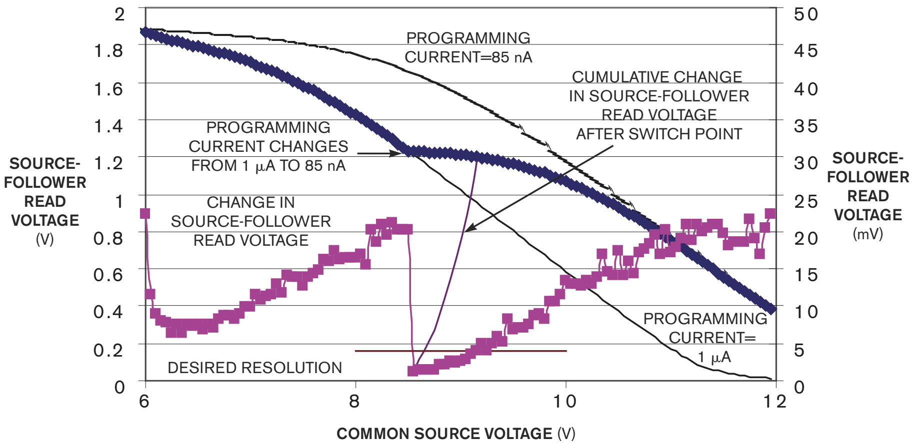


Figure 4 Programming an analog floating gate is complex. You must put repeated pulses on the programming gate and measure the results. This approach accommodates process variations (courtesy Nuvoton).

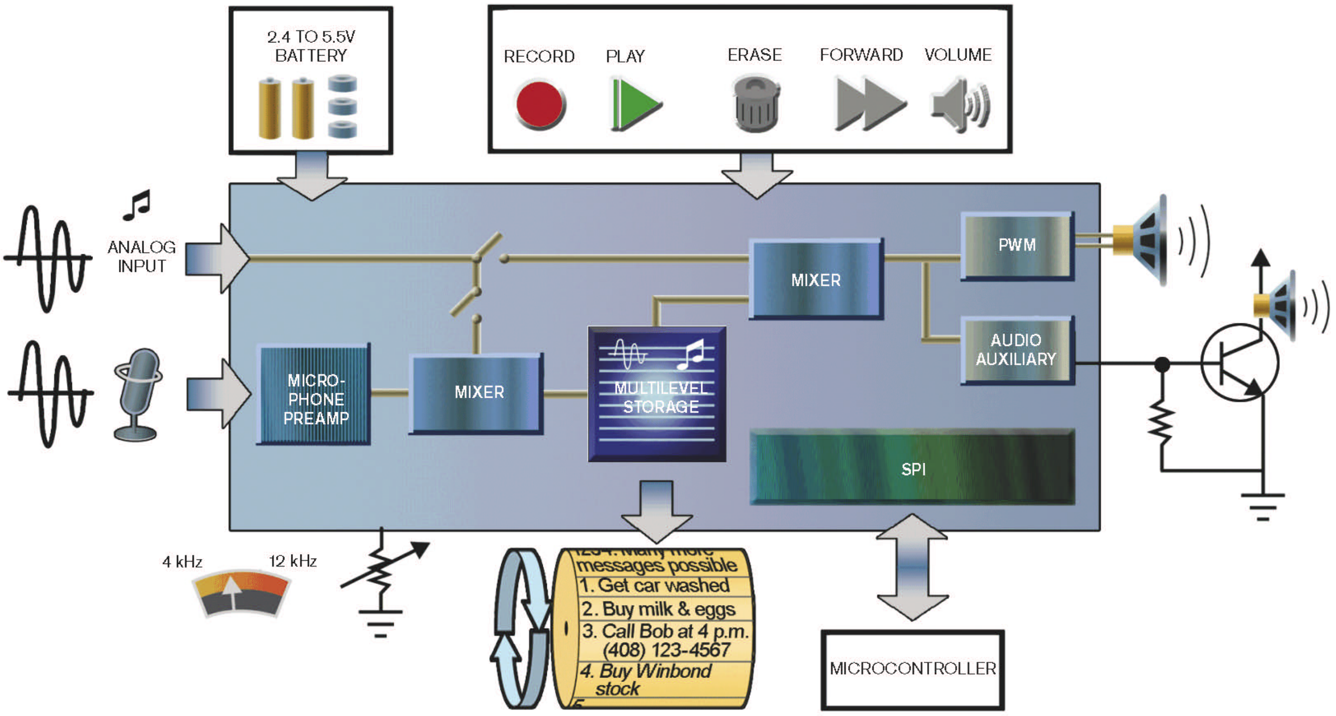


Figure 5 A floating-gate analog recording device is an entire system on a chip (courtesy Nuvoton).

Impinj had begun by 2005 to downplay its analog floating-gate technology and became a supplier of RFID (radio-frequency-identification)-tag silicon (**Reference 5**). By 2007, the company's engineers were writing articles that indicated it is more practical to use standard-logic CMOS floating-gate structures as digital storage devices (**Reference 6**).

This turnabout does not mean that analog floating-gate trimming structures are impractical. It does indicate, however, that if the use of a conventional fine-line CMOS is necessary to achieving your cost goals, you are better off using digital storage. Nevertheless, by acquiring Xicor in 2004, Intersil gained the expertise to offer a line of analog parts that uses floating gates to store an analog voltage. With a voltage reference, only one floating gate—the one that holds the part's reference voltage—is necessary. Because analog parts do not need the benefits of fine-line CMOS for smaller die, it is suitable to use a more complex CMOS process that has coarser line widths and more process steps to do the floating-gate structure. The die for a reference is small enough that the line-width penalty is not too severe.

Designers at Intersil can make the floating-gate structure in the voltage reference relatively large, allowing them to program the gate voltage to a precise level during manufacturing—a difficult task. "One benefit of floating-gate structures is that the temperature coefficient is substantially linear; it does not have a bow," easing temperature compensation, says Barry Harvey, a design fellow at Intersil. This linearity also means that you can program the gate to any voltage within reason, he adds. References using floating-gate structures have lower noise at smaller supply currents than do bandgap-based parts.

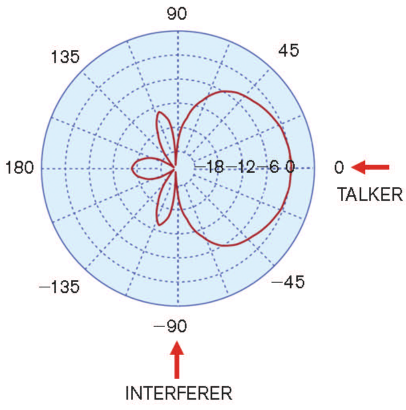


Figure 6 The GTX0050 cancels out noise from off-axis to a pair of microphones in GTronix's IR-reflow solderable module.

Intersil programs the parts in several steps. Further, the IC-design layout is complicated and prone to error, and package stress can affect the parts. "There are all these mobile ions in an IC process … really bad when you are storing charge on a floating gate," says Harvey. With clever design, process, and manufacturing, Intersil has overcome these problems. Few design tools are available to help designers craft a single floating-gate analog storage cell, so the engineers at Intersil had to spend considerable time and effort understanding the effects of process type and process variation on the devices' functions. Charge leaking off the gate is on the order of a few electrons per second, so the parts are suitable for decades of use, even at higher automotive temperatures (**Table 1**).

ANALOG PROCESSING

Several trade-offs in using an analog floating gate include whether you are using a fine-line CMOS process, the size of the die you are using, and the number of floating-gate storage cells your design requires. Another trade-off may make the use of floating gates especially desirable when you wish to keep your signal processing in the analog domain. Analog signal processing uses less power and has lower latency than its digital counterpart. Although digital signal processing has become ubiquitous, it involves a significant power penalty. You must digitize the signal, and the fast clock rates in the digital processing core use a lot of power. Further, you often must convert the signal back into the analog domain. A digital system can perform a 64-point FFT (fast Fourier transform) using 520 mW of power, whereas an analog signal-processing chip uses 13 mW. The analog die is also one-fifth the size of the digital die.

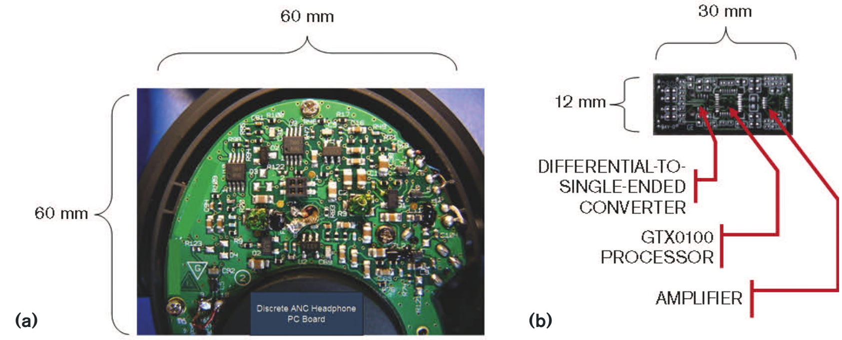


Figure 7 Using a discrete approach (a) takes up more space than using analog signal processing, as GTronix does with its GTX0050, which cancels out noise to a pair of headphones (b).

The fact that digital systems are, out of necessity, sampled-data systems gives rise to latency problems. These problems occur not just because of the delay necessary for taking a sample but also because digital signal processing uses filters that require digital feedback to locations in a shift register. The number of samples in that register dictate the latency that your system must suffer when you perform digital signal processing. In addition to higher power and long latency, the register requirements may require the storage of digital coefficients, so your CMOS process is more expensive because it must encompass EEPROM or flash-memory cells. For this reason, many DSP systems use an outboard EEPROM to store coefficients, allowing you to use silicon with the cheapest fine-line, logic-only CMOS process that has the smallest die and the fewest masks.

A pioneer in the use of analog signal processing, GTronix has licensed several patents from the Georgia Institute of Technology. Knowing that analog signal processing would be beneficial for battery-powered systems, GTronix has concentrated on designing parts for cell phones, mobile devices, and Bluetooth headsets. One product line includes chips for beam forming in mobile phones. The module combines two carefully spaced microphones and an analog signal-processing chip, allowing the phone to reject noise sources from the side and back (**Figure 6**). The tech-

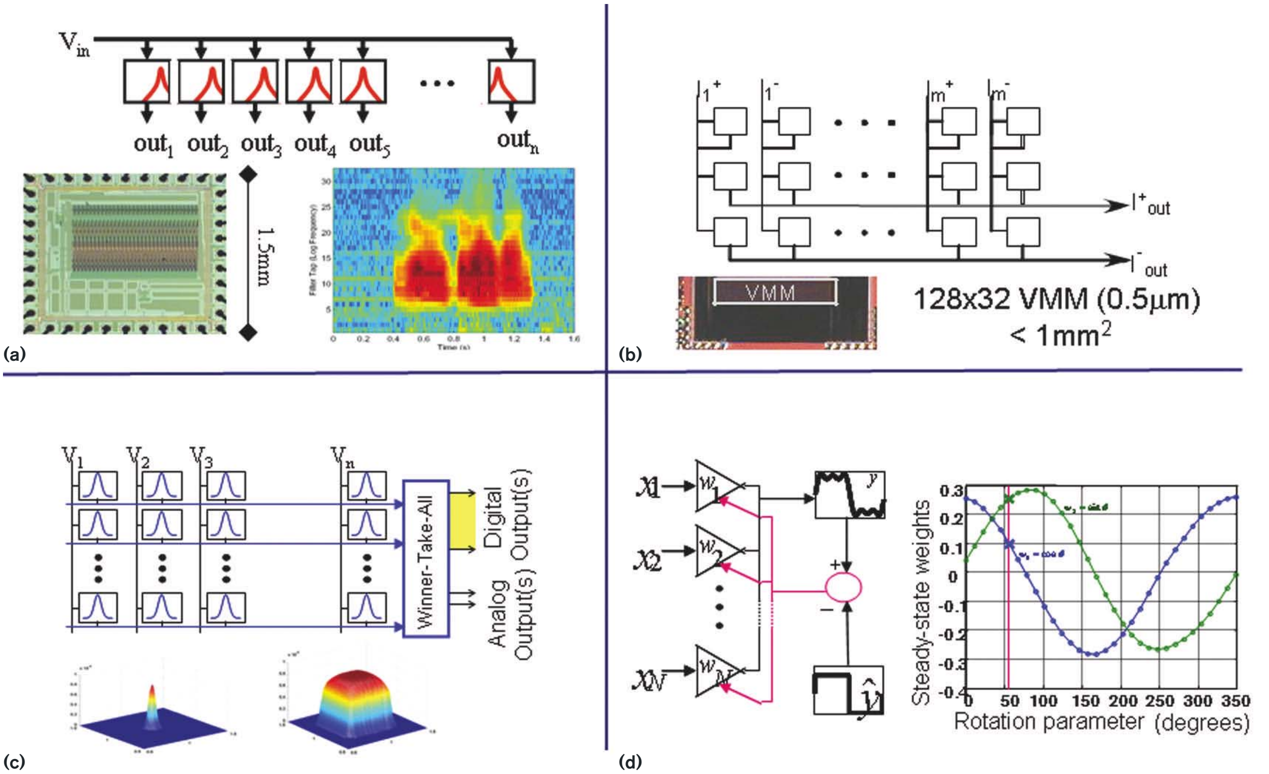
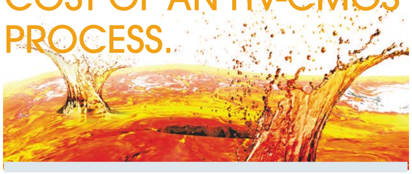


Figure 8 Analog floating gates allow signal processing in the analog domain, saving considerable power and reducing latency. Processing algorithms for constant-Q filter banks (a), vector-matrix multiplication (b), Gaussian-mixture models (c), and adaptive filters (d) are available to designers (courtesy GTronix).

nique yields significant improvements in clarity and reduction in background noise. The company is also pursuing active noise cancellation, such as that in today's consumer headphones. Although these headphones might already use analog techniques, the GTronix chip combines the analog functions into one chip, further reducing power (**Figure 7**).

ANALOG SIGNAL PROCESSING YIELDS ENOUGH BENEFITS TO JUSTIFY THE INCREASED COST OF AN HV-CMOS PROCESS.



Using floating-gate storage and analog signal processing, you can implement almost any signal-processing function (**Figure 8**). For example, you can design systems that perform DCTs (discrete cosine transforms), the mathematical basis for the compression that MP3 audio and JPEG images use. The only driving factor is that the application benefits from low latency and requires low power. Performing signal processing in the analog domain yields enough benefits to justify the increased cost of a CMOS process that has wider lines to support analog as well as more masks in production to make the floating-gate structures. If you have a large

TABLE 1 REPRESENTATIVE INTERSIL PARTS

Device	Output voltage (V)	Initial accuracy (mV)	Temperature coefficient (ppm/°C)	Maximum source current (µA)	Supply voltage (V)	Typical noise (µV p-p)	Minimum temperature (°C)	Maximum temperature (°C)	Stability (ppm)	Price (1000)	Package
ISL21032BPH306	0.6	±1	10	12	2.7 to 5.5	30	–40	130	10	$1.99	SOT-23
ISL21080DIH312	1.25	±7.5	50	1.5	2.7 to 5.5	30	–40	85	50	69 cents	SOT-23
ISL21007BFB825	2.5	±0.5	3	150	2.7 to 5.5	4.5	–40	125	50	$4.05	SOIC-8
ISL21060CFH633	3.3	±2.5	25	40	3.5 to 5.5	10	–40	125	100	95 cents	SOT-23
X60003C-41	4.096	±2.5	20	0.9	4.5 to 9	30	–40	85	10	$1.45	SOT-23

digital chip that supports flash memory, you may be better off doing your signal processing in digital, but there are more and more applications that benefit from removing functions from a large digital chip and putting them into specialized analog chips with process and power benefits. Today's small IC packaging enables this trend. You can thus add a small analog chip to your system with almost no penalty in the PCB (printed-circuit-board) area.

THE FUTURE

The future of analog floating-gate technology will bring further improvements in applications of audio storage, voltage references, and analog signal processing. Saleel Awsare, president of Nuvoton, sees applications in appliances and automotive, consumer, and medical devices. He envisions defibrillators that provide spoken instructions and smoke detectors that provide exit instructions, among others. Spoken warnings and instructions are far less distracting to drivers, so the chips have limitless potential in automotive applications. Hubert Engelbrechten, chief executive officer at GTronix, sees applications as diverse as glass-breaking detection, accelerometer signal processing, and medical-microsensor monitors. Researchers have also been looking at using analog floating gates as the building blocks for silicon that mimics the neural networks in brains (**references 7** and **8**). When you look at the function of the optic nerve, for example, you can see that the nerve is performing a significant amount of signal processing, greatly reducing the amount of information the eye sends to the brain. These functions are perfect applications for analog floating-gate structures because they can store processing coefficients in one silicon memory cell.

Spin-offs from neural research will give us many more applications for analog floating-gate technology in sensor signal conditioning. Ongoing research involves improving the accuracy and time required for programming a cell (**Reference 9**). Analog floating-gate technology may have taken decades to warm up, but it is sure to be a hot technology in the coming decade.**EDN**

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Precision equalization and test bring high-performance, low-cost cabling

THE HIGH DATA RATES OF COMMUNICATION PROTOCOLS MEAN TIGHT TIMING BUDGETS FOR THE COMMUNICATIONS CHANNEL, INCLUDING THE INTERCONNECTING COPPER CABLE. LOW-COST SIGNAL-CONDITIONING CIRCUITS AND CABLE-MEASUREMENT SYSTEMS CAN ADDRESS THIS PROBLEM BY CREATING RELIABLE, COST-EFFECTIVE CABLES FOR CONSUMER PRODUCTS.

The first step in understanding and allowing for electrical variations in low-cost cables is to establish a timing budget. The data rate sets the timing budget for the entire data channel. For example, a 3.4-Gbps channel has a bit time or UI (unit interval) and, hence, total budget of 294 psec. Designers must divide this budget among the receiver, the transmitter, and the interconnecting cable. The receiver requires an eye diagram with a 50%-open eye to adequately recover the data, thus using up half of the available budget. Transmitters are somewhat less budget-hungry. The random-jitter component of a transmitter with a state-of-the-art clock source would require 35 psec, or 12% of a UI at 3.4 Gbps. Other unavoidable deterministic sources of noise, such as clock-source duty-cycle distortion and power-supply noise, can increase the total transmitter budget until it makes up 30% of a UI. This amount leaves the cable with only 20% of a UI, or 60 psec for a 3.4-Gbps channel, to work with—a tough target by any standard.

PROCESS VARIATIONS

Low-cost copper cables are subject to significant electrical variation. One way to address this problem is to capture the quality of the data channel using analysis, such as insertion-loss measurement. **Figure 1** shows the result of insertion-loss measurement using a VNA (vector network analyzer). The analyzer measures the differential insertion loss over frequency of 32 passive, 5m AWG28 HDMI (high-definition-multimedia-interface) cables from the same bulk reel. The measurement analyzes the best cable, the worst cable, and an average cable from the batch. The differential insertion loss at the HDMI data frequency of 1.7 GHz for a 3.4-Gbps data channel ranges from −10 to −16 dB.

An alternative method of measuring cable performance uses an eye diagram, which takes into account all sources of signal degradation and presents them in a convenient form. Looking at eye diagrams makes it immediately obvious how much of the data-channel timing budget your design has consumed. Using an oscilloscope, you apply a fixed mathematical equalizer to each measurement before creating the eye diagrams. This equalizer gives a gain of approximately 10 dB at the data frequency to the signal. Without this gain, all of the eyes would remain closed, meaning that you would be unable to discern relative channel quality.

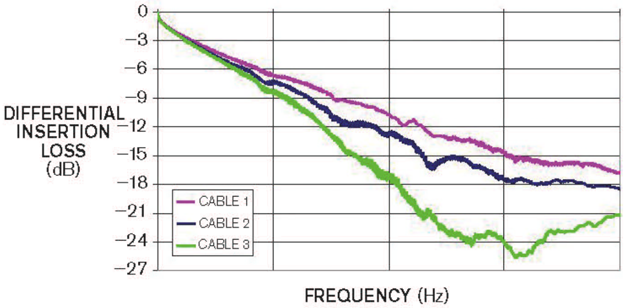

Figure 1 A vector network analyzer measures differential insertion loss over frequency for the best cable, the worst cable, and an average cable from a batch of 32 5m AWG28 passive HDMI cables from the same bulk reel.

From the plots in **Figure 2**, you can clearly see that significant eye degradation occurs between Cable 1 with −10-dB insertion loss and Cable 3 with −16-dB insertion loss (**Figure 2a**). The eye mask is set for a receiver requiring a 50% eye opening. Cable 1 and the transmitter show a high-quality open eye with no eye-mask violations. The transmitter is a laboratory data-pattern generator with low noise sources, using approximately 10% of the timing budget. Cable 2 and the same transmitter have some eye-mask violations; hence, there may be errors in the received signal (**Figure 2b**). Cable 3 and the same transmitter have significant eye-mask violations and hence a completely unrecoverable signal (**Figure 2c**).

Now consider the reasons for the electrical eye variations in this batch of cables in the context of the steps involved in cable production. Step 1 is to make an insulated copper core. As with any manufacturing process, the material properties and physical dimensions of the copper and the insulator have an average value and tolerances on the order of ±10%.

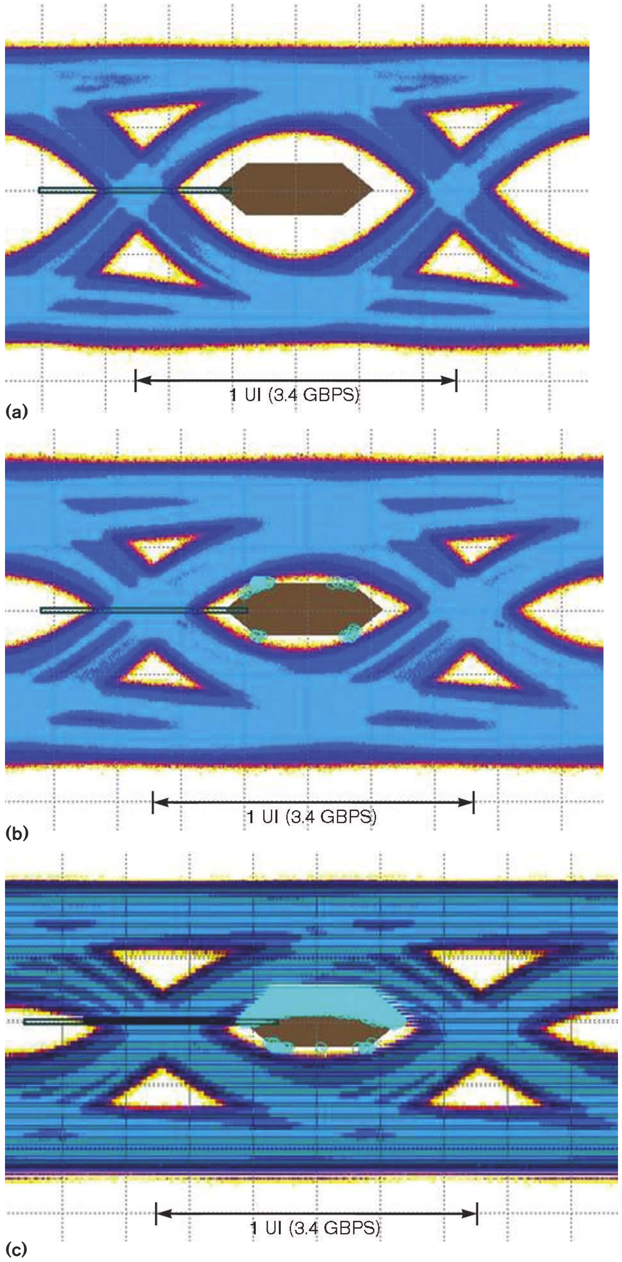

Figure 2 Eye diagrams for cables 1, 2, and 3, respectively, show a high-quality open eye with no eye mask (the black hexagon in the middle of the eye) and −10-dB insertion loss (a); some eye-mask violations, indicating there may be errors in the received signal and −12-dB insertion loss (b); and significant eye-mask violations with a completely unrecoverable signal and −16-dB insertion loss (c).

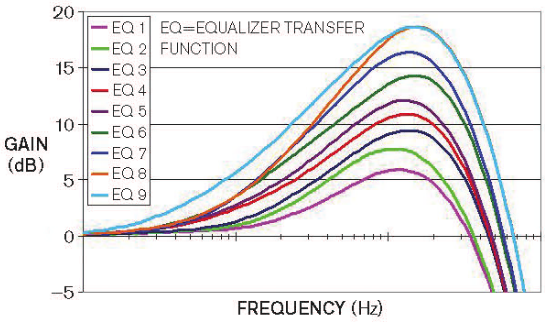

Figure 3 Equalizer transfer functions have successively increasing gain levels.

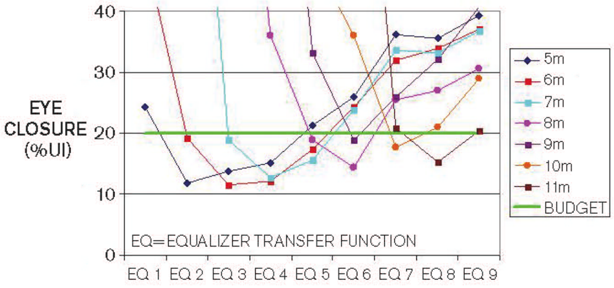

Figure 4 You can use equalizer transfer functions to equalize increasing lengths of AWG32 cable.

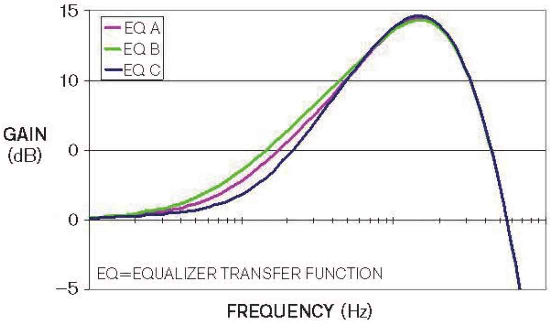

Figure 5 Equalizer transfer characteristics have different gains with different low-frequency characteristics.

The material properties and physical dimensions vary along the cable's length. This variation in turn causes variations in conductivity, permittivity, and permeability. At a higher level, these electrical properties affect cable parameters, such as characteristic impedance and attenuation profile. Variability in these properties directly affects the electrical eye.

Step 2 is to create a differential pair, usually by twisting two insulated cores around each other. The twisting technique makes the distance between the cores both small and consistent, which helps control the differential characteristic impedance and reduces the electromagnetic emissions from the pair. This technique's lack of precise control, however, can lead to intrapair skew—a significant contributor to electrical eye variability—due to a difference in length between the two component wires. In some cases, twisting the cables more slowly can improve this length mismatch. However, this

Figure 6 You can use equalizer transfer functions to equalize two channels of an 8m AWG32 cable. EQ A is a reasonable but not optimal choice for Channel 2, EQ C is the best transfer function for Channel 1, and EQ B is the best transfer function for Channel 2.

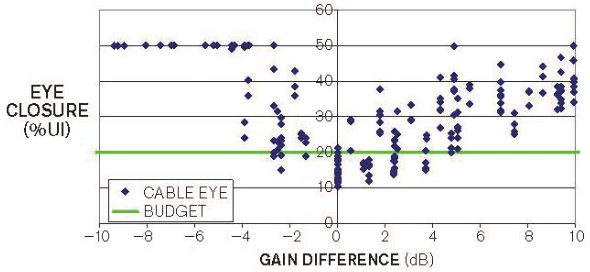

Figure 7 Accurate signal conditioning and eye measurement result in high cable yield.

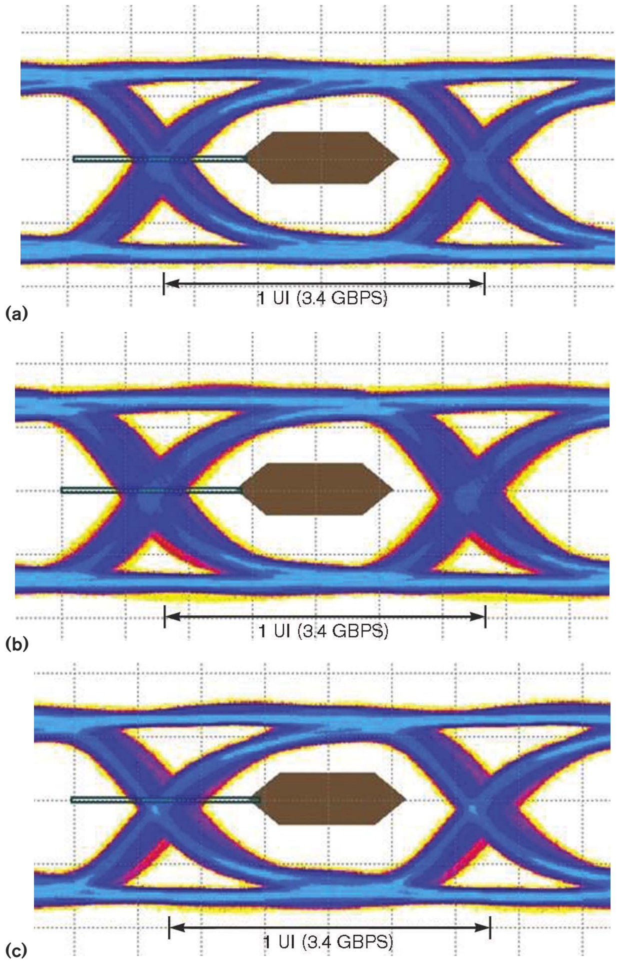

Figure 8 With the application of tuned equalization to each cable output for the same three cables as those in figures 2a, b, and c, respectively, but with the application of tuned equalization to each cable output, all the cables now have high-quality eyes with no mask violations.

approach results in longer production times and so creates the need to trade off cost versus quality.

Step 3 is to assemble the bulk cable with the required number of pairs and cores, which loosely wrap around each other along the cable length. Adjacent signal pairs typically have some crosstalk. Both physical proximity and the presence or absence of electromagnetic shielding between the wires affect crosstalk. Choosing the quality and thickness of the shield is also a cost-versus-quality trade-off in cable production.

Step 4 is the connection or termination of the bulk cable to the connector. Termination involves stripping back a certain amount of shielding and insulation to gain access to the bare conductors. This lack of insulation and shielding, even over short distances, can cause significant characteristic impedance variation and an increase in crosstalk, both of which cause variation in the electrical eye. Minimization and control of the strip-back distance help to reduce these problems. A further source variation occurs when you solder each wire to the connector. You must design the impedance of the solder-fillet form making the contact to avoid an impedance discontinuity. In designing the processes necessary for terminating a bulk cable, the manufacturer must trade off cost versus quality.

In short, manufacturers must perform a number of steps in the production of a cable, and each step requires precision to maximize signal integrity. In volume production, however, the parameters in each process step vary to some degree, and all of these fluctuations combine to cause variation in eye quality.

SIGNAL CONDITIONING

Cable-process data clearly shows that each channel within a cable may differ due to process variations and hence may require different levels of signal conditioning to sufficiently re-create the signal. The signaling-conditioning circuit, or equalizer, applies an approximation of the inverse of the cable-loss characteristic at the output of the cable. The first step in designing an equalizer for a cable is to produce a filter-transfer function that has a gain at the data frequency that is equivalent to the cable loss at the data frequency. **Figure 3** shows a range of equalizer transfer functions that gives increasing gain at the data frequency. **Figure 4** shows how you can use each of these equalizer transfer functions to equalize increasing lengths of AWG32 cable. Designers can make these measurements using an oscilloscope, a tunable equalizer, and cables that represent the mean parameters of the batch. The **figure** illustrates an optimal gain level for each cable length; selecting any gain level above or below this level causes a degradation in performance. Thus, you need some method of selecting this optimal equalizer gain level for a cable.

Important criteria for this selection include the gain level not only at the data frequency but also at lower frequencies. **Figure 5** shows three equalizer transfer characteristics with the same gain at the data frequency but with gains that differ by as much as 2 dB at one-tenth of the data rate. The lowest frequency of interest depends on the longest run of the data stream. An 8b/10b data stream has a maximum run length of five, whereas an HDMI data stream typically has a maximum run length of 11. This length places greater demands on the equalization function. **Figure 6** shows how you can use these equalizer transfer functions to equalize two channels of an 8m AWG32 cable. EQ A is a reasonable but not optimal choice for Channel 2, EQ C is the best transfer function for Channel 1, and EQ B is the best transfer function for Channel 2. Thus, relatively subtle changes of equalizer characteristic can affect the performance of this cable. This situation emphasizes the need for both careful equalizer-characteristic selection and the availability of a wide range of equalizer characteristics to maintain end-product performance.

Given the wide process spread across low-cost, high-volume, and high-data-rate cables, how does the manufacturer guarantee the quality of every cable? Low-speed, low-cost, high-volume cable products—USB (Universal Serial Bus) 2.0, for example—traditionally used statistical process control to guarantee cable performance. **Figure 2** shows the drawbacks of this method. In the higher-priced enterprise markets, expensive and time-consuming oscilloscope-based systems can be used to test the cables. Consumer products cannot afford such test systems. A purpose-built tester is thus required. The criteria for this tester are low cost; accuracy, ideally to ±5 psec; and speed of less than 1 sec per cable. With this accuracy and speed achieved, it is trivial to check a range of equalizer characteristics to find the optimum setting. A simple user interface and mechanical robustness make it compatible with the production environments for such cables.

Figure 7 shows the result of running a custom-built in-house tester across a range of 27 cables of various lengths and quantities. The 0-dB point on the X axis is the best equalization filter available. As you move toward the left along the graph's X axis, you'll see that the signal is underequalized; as you move toward the right along the X axis, the signal is overequalized. Thus, good equalizer selection significantly improves the cable yield, and the ability to measure the cable eye ensures the quality of the shipped product. **Figures 8a**, **b**, and **c** show the oscilloscope-measured eye diagrams for the same three cables as those in **Figure 2** but with the application of tuned equalization to each cable output. Each cable requires a different level of equalization, and all the cables now have high-quality eyes with no mask violations.**EDN**

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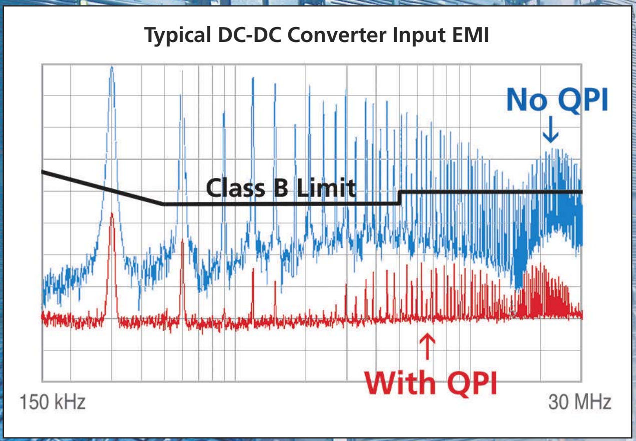

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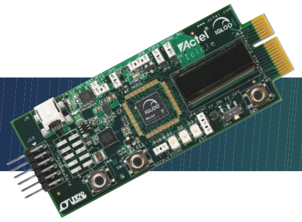

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Compact, four-quadrant lock-in amplifier generates two analog outputs

Stefano Salvatori and Marco Girolami,
Università Degli Studi Roma Tre, Rome, Italy

The circuit in this Design Idea realizes a simple, low-cost lock-in amplifier employing an Analog Devices (www.analog.com) AD630 balanced modulator-demodulator IC (**Reference 1**). The device uses laser-trimmed thin-film resistors, yielding accuracy and stability and, thus, a flexible commutation architecture. It finds use in sophisticated signal-processing applications, including synchronous detection. The amplifier can detect a weak ac signal even in the presence of noise sources of much greater amplitude when you know the signal's frequency and phase.

As an analog multiplier, the AD630 reveals the component of the input-voltage signal in a narrow band around the frequency of the reference signal. The lowpass filter at the AD630's output allows you to gain information on the weak signal amplitude, which the uncorrelated noise originally masked. When the input voltage and the reference voltage are in phase, the lowpass filter's output, V_{OUT}, assumes the maximum amplitude. Conversely, if the input voltage and the reference voltage are in quadrature, the output voltage would ideally be 0V. In this way, if both in-phase and quadrature reference signals are available, two balanced demodulators reveal the in-phase output voltage to be 0° and the in-quadrature output voltage to be 90°. You can calculate the module and phase shift as follows:

$$|V_{OUT}| = \sqrt{V^2_{OUT0°} + V^2_{OUT90°}};$$

$$\angle V_{OUT} = \tan^{-1}\left(\frac{V_{OUT90°}}{V_{OUT0°}}\right).$$

The two AD630s have a gain of ±2 and receive the amplified signal, V_{IN}, through two identical amplifiers, A_1 and A_2. At Pin 7 of IC_1, a bipolar ±5V squared signal appears in phase with

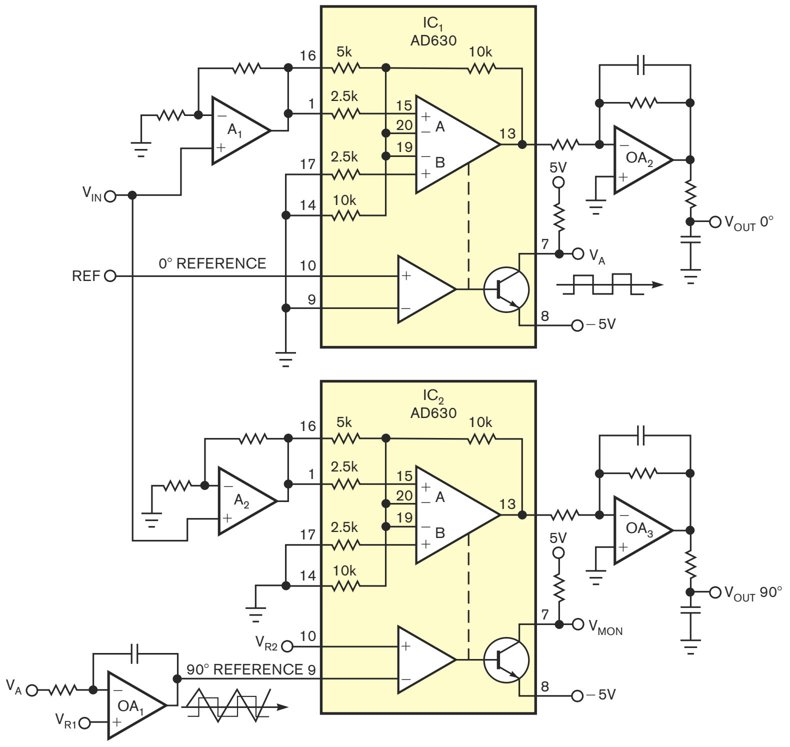

Figure 1 OA_1 integrates the bipolar V_A signal and creates a triangular wave. V_{R1} and V_{R2} obtain a 90°-shifted reference voltage with respect to V_A.

the reference signal. OA_1 integrates the amplifier voltage, which generates a triangular wave that IC_2's comparator compares with the V_{R2} voltage. You must regulate V_{R1} and V_{R2} to obtain a perfect 90°-shifted command for IC_2. You can monitor the voltage at IC_2's Pin 7. Measurement accuracy and repeatability depend strongly on the RC time constant of the integrator and the values of V_{R1} and V_{R2}.

You can use a different approach to generate in-phase and in-quadrature reference signals. **Figure 2** shows an all-digital circuit, which you can implement in a small CPLD (complex programmable-logic device) to generate the 0 and 90° reference signals in **Figure 1**. Counter 1 measures the reference-signal time in terms of the N number of digital clock pulses, where the reference time can be different from 50%. It receives a preset command at the $N_1=1$ value at each positive front edge of the reference signal. D-type flip-flop IC_1 generates such pulses. At each positive edge of the reference signal, IC_2 acquires the N/4 value. Meanwhile, Counter 2 counts the clock periods and receives a restart command at the $N_2=1$ value when its value reaches the comparator-measured N/4 quantity.

AN INCREASE IN THE NUMBER OF BITS DECREASES THE MAXIMUM REFERENCE FREQUENCY.

To overcome the lack of the last EQ signal when the reference time is greater than approximately four times the N/4 integer value, the OR combination of the two RST and EQ pulses yields four almost-equidistant positive-edge commands in each reference-time period. The N/4 integer division, a logical right shift by 2 bits of N_1, gives a maximum error of three on the last pulse position. These pulses generate the in-phase and in-quadrature signals, 0 and 90°, respectively, resulting from simple commutations on the positive or negative edges of the signal. T-type flip-flop IC_3 generates a signal with twice the frequency of the reference signal. In this way, the accuracy is equal to $3/N_1$.

To maintain accuracy at least comparable with that of the AD630, the N_1 output of Counter 1 would be the highest. However, an increase in the number of bits decreases the maximum reference frequency for a given digital-clock frequency if you want N_1 to reach high values. For example, if N is 15 bits, the N_1 output assumes the 32,767 maximum value with an accuracy of approximately 0.01%. If the reference-time period decreases, you can assume a minimum value of 3277—that is, one-tenth of the maximum value—for N_1, with a correspondingly lower accuracy of 0.1%, which is comparable to the gain accuracy of the AD630. To increase the reference frequency, divide the digital clock's frequency to select low values when the reference time becomes too long. **EDN**

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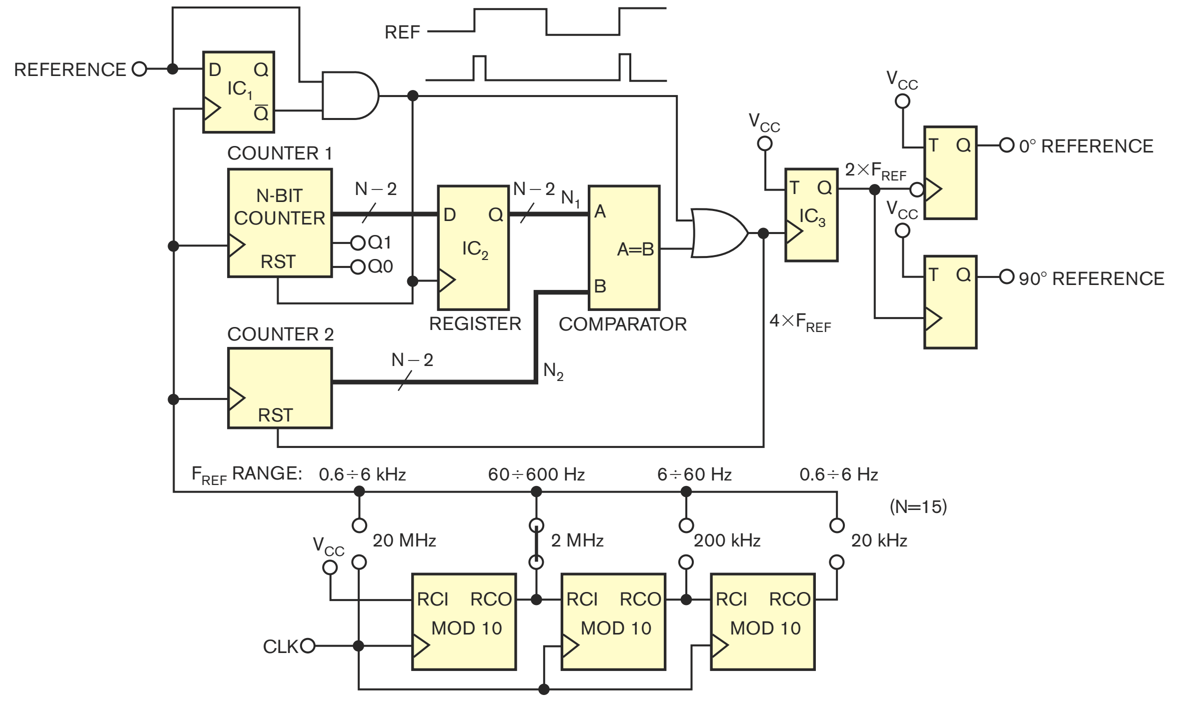

Figure 2 You can implement this all-digital circuit in a small CPLD.

Eight-function remote uses one button, no microcode

Jay Davis, Boeing Integrated Defense Systems, Wichita, KS

Many people with significant physical disabilities can't operate everyday mechanisms, such as TV remote controls. To make matters worse, adaptive technologies are often unaffordable unless insurance covers them. This Design Idea describes an interface circuit that lets a disabled person control eight remote-control functions. The design uses older, small-scale-integration ICs because of their simplicity, low power requirements, affordability, and availability at stores such as Radio Shack (www.radioshack.com). Because the circuit uses no microcontroller, you need not do any programming.

Power for the circuit in **Figure 1** comes from four 1.5V AA batteries in series. Diodes D_1 through D_4 reduce the battery power from 6V to approximately 3.4V, and they protect against accidental reverse polarity of the batteries. IC_1, a 555 timer, and associated discrete components form a repetitive-pulse generator. Potentiometer R_1 adjusts the pulse speed. This pulse feeds directly into decade counter, IC_2, which causes indicator LEDs LED_1 through LED_4 to sequence on and off. Each output of the decade counter feeds one input of CMOS gate IC_3 and AND gate IC_4.

Normally, the output of the NAND gate is low because both inputs must be logic one to produce a logic-one output to close one of the CMOS switches, IC_5 and IC_6.

If the user presses the control switch while the desired LED is lit, both inputs to one of IC_3's AND gates are at logic one, causing the output to be logic one and closing a 4066 switch, which is effectively the same as pressing one of the buttons on the remote control. As long as the control switch remains closed, the 555 pulses remain disabled and LED_1 through LED_4 remain in their current state. This characteristic is important because a person can continue to hold the control switch closed to continuously increment the changing of a channel or increase or decrease the volume.EDN

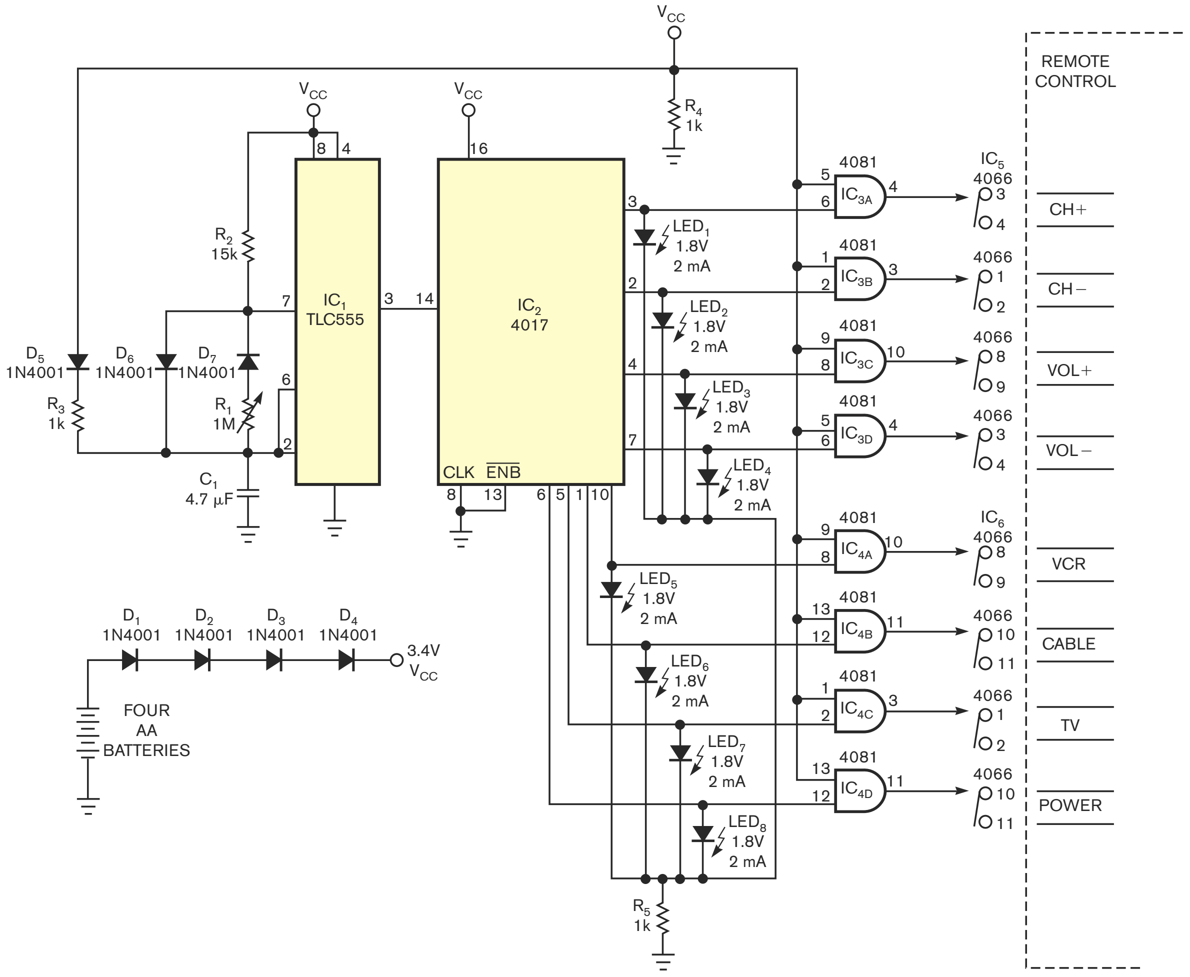

Figure 1 This interface circuit allows a disabled person to control eight remote-control functions.

Doorbell transformer acts as simple water-leak detector

Jeff Tregre, www.BuildingUltimateModels.com, Dallas, TX

Shortly after installation, the simple water-leak-detector circuit in this Design Idea saved the day and hundreds of dollars. The average life expectancy of a hot-water heater is about 10 years. It's not a question of whether it will leak; it is simply a matter of when it will leak. The builders of new homes in the Midsouth region of the United States have been installing hot-water heaters in attics. This approach saves valuable space; however, if you only infrequently visit the attic, you may not discover that your hot-water heater is leaking until it is too late. By that time, it may cost you hundreds of dollars to repair the water damage to ceilings and walls.

The circuit in **Figure 1** detects hot-water-heater leakage, and you can also use it for detecting leaks in dishwashers, garbage disposals, ice makers, swimming pools, hot tubs, and waterbeds. **Figure 2** shows the completed circuit.

Most doorbell transformers produce

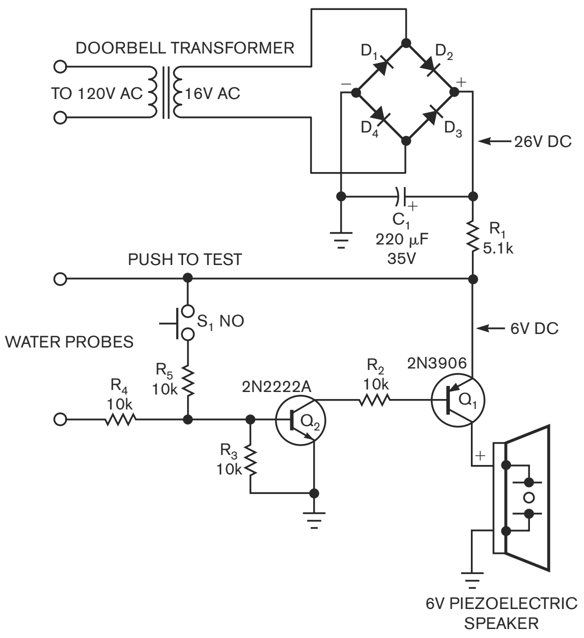

Figure 1 A transformer and a bridge provide power for the speaker.

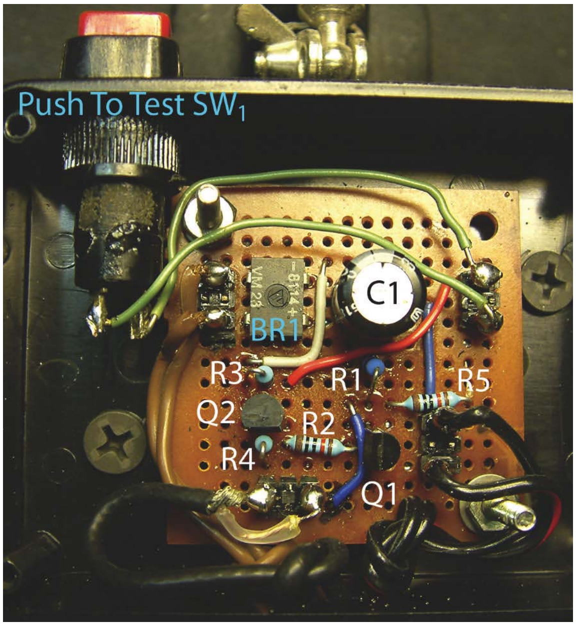

Figure 2 The circuit includes a push-to-test button.

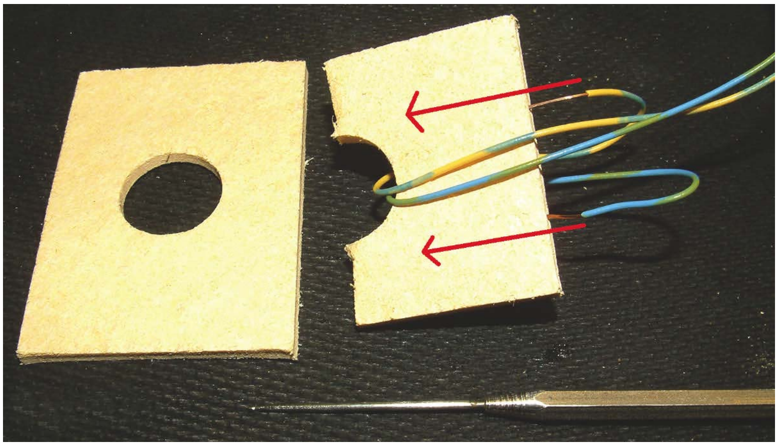

Figure 3 Use a sponge and copper wire to form a water probe.

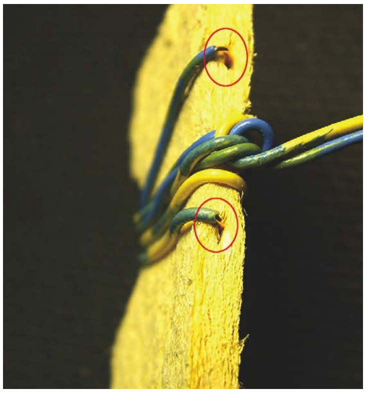

Figure 4 The completed probe with bare wire inside senses water through a change in resistance.

16 to 20V ac. To drive the buzzer, you must convert the ac voltage to dc: Multiply the ac voltage by 1.414 to yield the dc-rms voltage. Connect the wires to the secondary side of the transformer to a bridge rectifier and then into a filtering electrolytic capacitor. Your power supply should now be providing about 26V dc. The 5.1-kΩ resistor, R_1, limits the current to the buzzer. When the system detects water or when you press the push-to-test switch, you have about 6V dc to operate the circuit and sound the piezoelectric speaker. Mount the speaker so that you'll hear it when it sounds.

Transistors Q_1 and Q_2 can be any general-purpose NPN and PNP types, respectively. The water probes use copper wires about 1 in. apart from each other. You then pierce two holes, about 1 in. apart, into a sponge from a soldering station. Insert bare copper wire into these holes (**Figure 3**). Take some of the remaining wire but leave the insulation on it and wrap it around the sponge so that the bare copper wire does not come out (**Figure 4**).

You can now place this sponge in the metal overflow tray underneath the hot-water heater. When the hot water leaks, the sponge absorbs it. The resistance between the two bare copper wires then drops to about 1 MΩ or less, which forward-biases the two transistors and enables the piezoelectric speaker. The cost for this circuit shouldn't exceed $25. If you have more than one hot-water heater in the same area, you can make another water probe and tie the two probes together in parallel.**EDN**

Inverted regulator increases choice and reduces complexity

David McCracken, Aptos, CA

Most circuits are referenced to ground, where relatively low-voltage components can monitor and control the low side of a load but not the high side. For example, nearly any low-voltage rail-to-rail-input op amp can detect a voltage increase indicating overcurrent through a resistor that connects between the load and ground. To do the same thing on the high side, you typically select a differential amplifier that tolerates high common-mode voltage. This approach limits the component choices for the

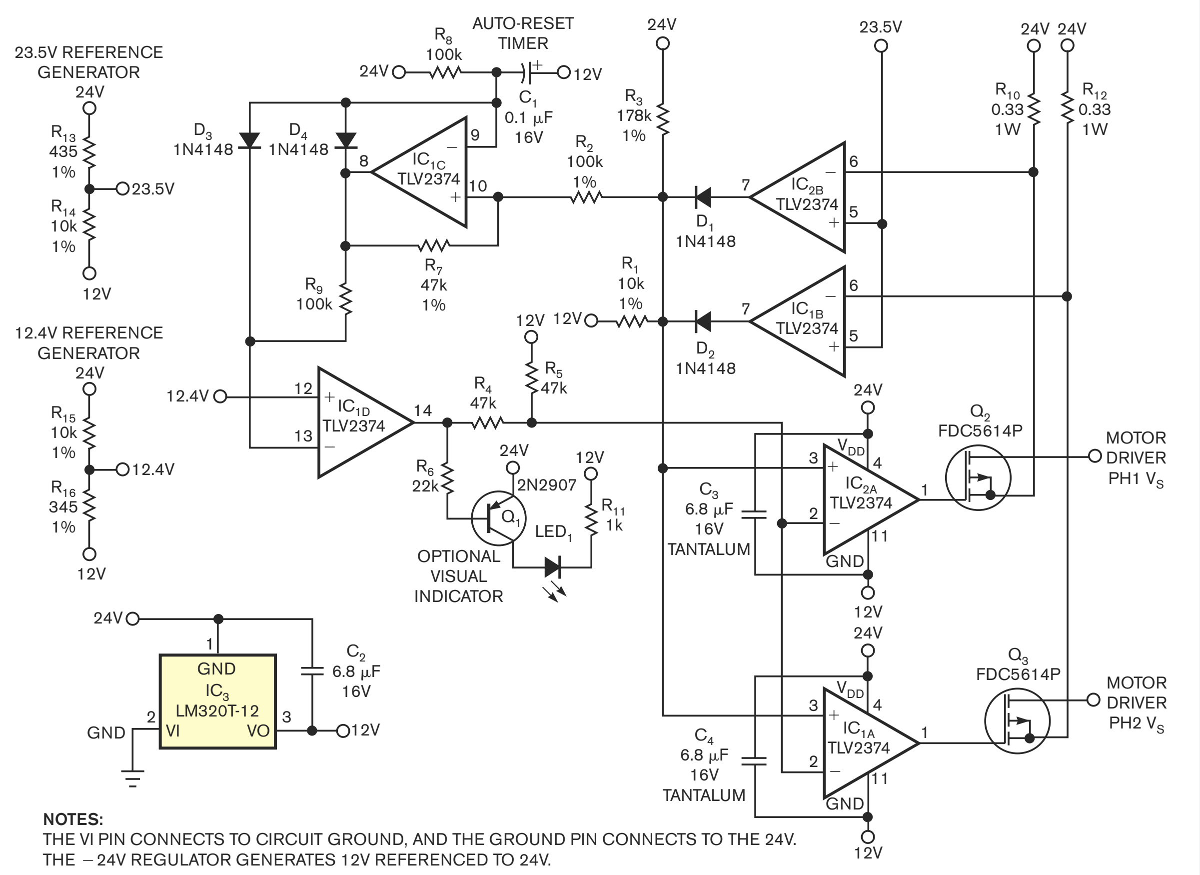

Figure 1 Current-sense resistors turn off MOSFETs when current through them exceeds a limit.

input amplifier and brings up the question of how to respond to an overcurrent. The differential amp produces a low ground-referenced signal from a high-side event, but you can prevent a high-side overcurrent resulting from a short to ground only by turning off the high-side power. In effect, the differential amp translates the high-side signal into the low-side domain in which you must then translate the response back into the high-side domain.

A simpler approach for any high-side overcurrent-protection circuit references the entire circuit to the high-side rail. Such circuits typically consume little power, which a small, three-terminal linear regulator can easily supply. However, this approach requires an unusual configuration employing a negative regulator whose ground pin connects to the high-side rail and whose input connects to system ground. There are no other connections to system ground. All "ground" points of the overcurrent-protection circuit connect to the regulator's out pin.

Figure 1 shows a two-phase-stepper-motor, fast-acting, self-resetting high-side circuit breaker with a 24V power supply to the motor and a 12V power supply to the circuit breaker that is referenced to 24V. The circuit breaker sees the 24V motor's power rail as 12V referenced to its local ground, which the regulator's output provides. Like all negative linear regulators, the circuit requires a 6.8-μF tantalum capacitor.

R_{10} and R_{12}, both 0.33Ω, 1W resistors, provide current sensing for the two phases. High-side power flows through a sense resistor and a P-channel MOSFET to the high-side input of an H bridge (not shown), which drives one motor winding. Current in either phase can cause the sense voltage to increase to 0.5V, triggering the breaker. The circuit responds by turning off both MOSFETs. It then waits 20 msec and turns them back on, automatically clearing momentary shorts.**EDN**

Debug a microcontroller-to-FPGA interface from the FPGA side

Bibo Yang, Sunrise Telecom, Beijing, China

Microcontrollers and FPGAs often work together in embedded systems. As more functions move into the FPGA, however, debugging the interface between the two devices becomes more difficult. The traditional debugging approach comes from the microcontroller side, which relies on a serial-port printout. This approach adds overhead and may cause timing problems. Furthermore, this approach cannot guarantee uninterrupted and exclusive access to certain addresses because of operating-system multitasking. Thus, a serial-port printout doesn't accurately describe the actions on the microcontroller/FPGA interface.

Instead, you can approach the problem from the FPGA side using a JTAG (Joint Test Action Group) interface as a communication port. This approach uses the internal logic of the FPGA to capture the read/write transactions on the microcontroller/FPGA interface. This method is nonintrusive because the circuit that captures transactions sits between the microcontroller and the FPGA's functioning logic and monitors the data without interfering with it. It stores the captured transaction in the FPGA's RAM resources in real time. You can transfer the data to a PC through the JTAG port's download cable.

The debugging tool comprises the data-capture circuit, the JTAG communication circuit, and the GUI (graphical user interface). The data-capture circuit uses standard HDL (hardware-description language) and instantiates a FIFO (first-in/first-out) buffer in the FPGA. Whenever you read or write to a register, the debugging tool records the corresponding value of the address and data on the bus and stores it in the FIFO buffer. You can retrieve the data through the JTAG's download cable to the PC (**Listing 1**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

Because the FPGA has limited on-chip RAM resources, you must keep the FIFO buffer shallow. To efficiently use the FIFO buffer, the design includes filter and trigger circuits. With inclusive address filtering, the circuit monitors only several discontinuous spans of addresses instead of the whole address space. Exclusive-address filters can filter out several smaller address spans from the inclusive-address spans, enabling finer control of the filter settings (**Listing 2**, which is also available in the online version of this Design Idea at www.edn.com/091215dia).

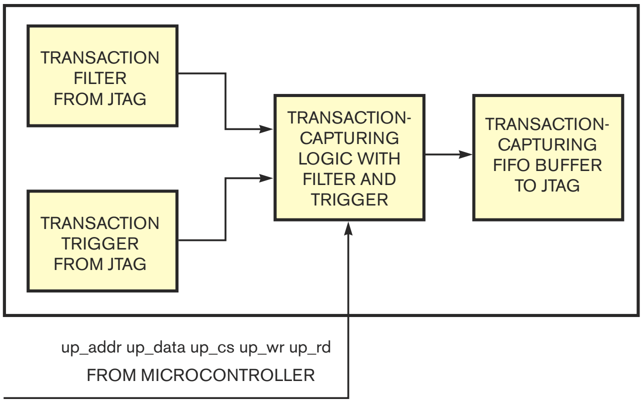

Figure 1 The JTAG's vendor-supplied, customizable communication circuit has two interfaces.

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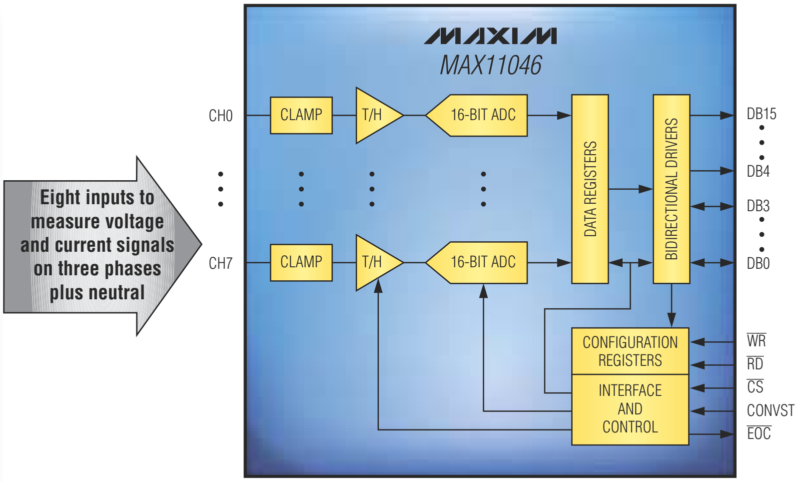

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With transaction triggering, the circuit starts when you read from or write to a certain address. You can add certain data values to the triggering condition (**Listing 3**, which is available in the online version of this Design Idea at www.edn.com/091215dia). You can dynamically reconfigure the settings of address filters and transaction triggers through the JTAG's vendor-supplied, customizable communication circuit without recompilation of the FPGA design (**Figure 1**). The circuit has two interfaces, one of which is written in HDL to form a customized JTAG chain. It communicates with the user logic (**listings 1**, **2**, and **3**). The circuit is accessible through specific programming interfaces on the PC and communicates with the user program or GUI (**Listing 4**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

The FPGA-based circuit facilitates writing and reading functions from PC to FPGA logic, and it promotes the JTAG interface to a general communication port attached to the FPGA. FPGA manufacturers, including Actel (www.actel.com), Altera (www.altera.com), Lattice Semiconductor (www.latticesemi.com), and Xilinx (www.xilinx.com), respectively, call this circuit UJTAG (user JTAG), Virtual JTAG, ORCAstra, and BScan (**references 1** through **4**).

The GUI for this circuit uses Tcl/Tk (tool-command-language tool kit). FPGA manufacturers provide vendor-specific APIs (application-programming interfaces) in Tcl for the PC side of the JTAG-communication circuit. The APIs include basic functions, such as JTAG-chain initialization, selection, and data reading and writing. With the data-read function, you can check the capturing status and get the transaction data from the FIFO buffer. With the data-writing function, you can send the filter and trigger configuration data to the capturing circuit in the FPGA (**Listing 4**). The JTAG-based debugging method provides dynamic visibility and controllability into the microcontroller-to-FPGA interface and the FPGA's internal logic without the need to recompile and download FPGA code.**EDN**

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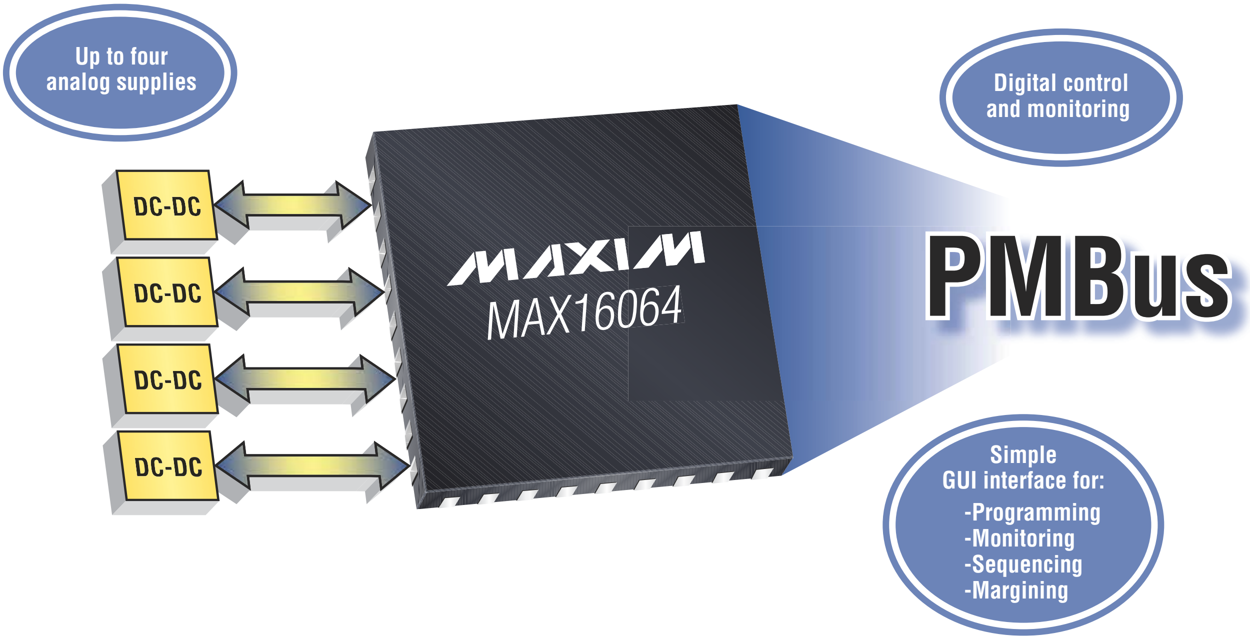

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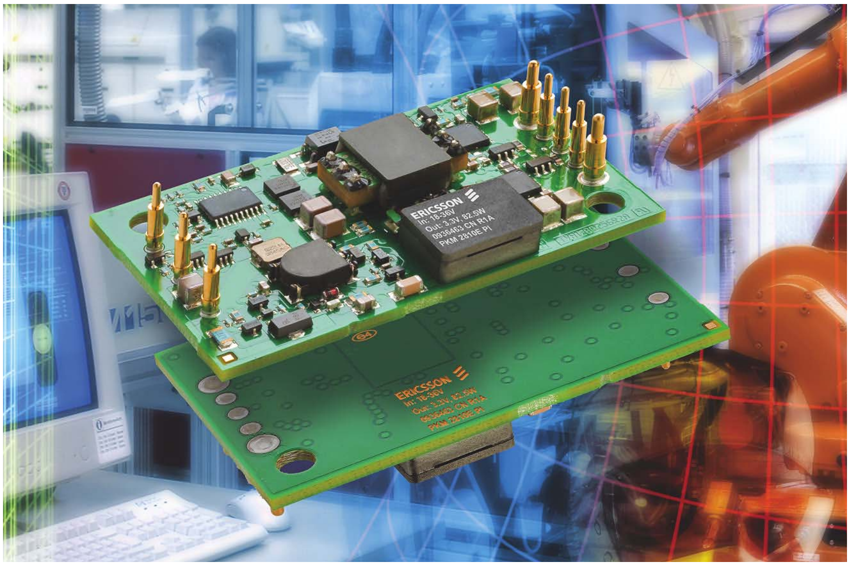

24V module weighs 25g

The 24V input PKM2810EPI dc/dc module claims 92.5% efficiency at half-load and 89.5% efficiency at full load. Aiming at telecom systems requiring 24V batteries, the device accepts 18 to 36V input voltages. The 25g device also suits use in process-control, automation, robotic, and transportation applications. The module costs $23.

Ericsson, www.ericsson.com

DC/DC converter uses galvanic isolation to reduce switching noise

The MER1 dc/dc converter provides local power on control-system boards and other applications that cannot tolerate wide output-voltage variations. UL 60950 certification is pending for the performance-isolated, 1W, single-output device. Five input voltages range from 5 to 48V, and output voltages are 5, 9, 12, or 15V. The device operates over a −40 to +85°C temperature range and provides typical efficiency of 89%. Galvanic isolation of 1 kV dc reduces switching noise. Available in a 19.65×6.15×10.15-mm package, the converter costs $4.20.

Murata Power Solutions, www.murata-ps.com

Half-brick dc/dc converter targets use in RF amplifiers

Suiting cellular-infrastructure applications, such as RF amplifiers, the 350W HBA48T12280 half-brick dc/dc converter claims a 90% or higher efficiency for loading conditions from 40 to 100%. The converter operates within a 21 to 33V-dc output. Features include a 36 to 75V-dc input range, a −40 to +100°C temperature range, and the ability to withstand a 100V input transient for 100 msec. The HBA48T12280 costs $49 (1000).

Power-One, www.power-one.com

100W power supply has high power density

Meeting industrial- and medical-safety standards, the single-output 100W ECS100 ac/dc power supply provides a 10.4W/in.^{3} power density, fitting into a 1U space. The units provide 80W when convection-cooled and require 10 cfm of forced airflow, providing a 100W full output. Claiming 88% typical efficiency, the power supply has a −20 to +70°C operating temperature with derating from 50°C. Available in a 2×4×1.2-in. package with a metal-cover option, the 100W ECS100 ac/dc power supply costs $45.24.

XP Power, www.xppower.com

DIN rail-mount power supplies use three-phase ac inputs

The DPP120, DPP240, and DPP480 ac/dc DIN rail-mount power supplies operate off a three-phase ac-line input from 340 to 575V ac. The DPP120 series has 12 and 24V-dc output voltages at 120W, and the 240W DPP240 series and 480W DPP480 series provide 24 and 48V-dc output voltages. A bi-phase-operation feature allows continuous operation with the output power derated to 80% under dropped-phase conditions. The devices provide power-factor correction in accordance with EN61000-3-2. Additional features include an adjustable output voltage, allowing voltage drops in cables, and a ±1% load regulation when

POWER SOURCES

the supplies are used individually and ±5% when two supplies are connected in parallel for higher-power applications. The DPP120-, DPP240-, and DPP480-series ac/dc DIN rail-mount power supplies cost $64 (1000).
TDK-Lambda, www.us.tdk-lambda.com/lp

INTEGRATED CIRCUITS

Transceiver meets FlexRay Version 2.1 Revision B specifications

Complying with the latest FlexRay Version 2.1 Revision B standard, the AS8221 FlexRay transceiver acts as the interface between digital logic and copper-cable transmission. Features include 10-Mbps transmission rates, a short asymmetric delay, and an interface allowing optional monitoring of circuits. In a fault condition, the circuit-monitoring feature can uncouple the control unit from the communication network. Aiming at automotive applications, the product operates over a −40 to +125°C extended-temperature range. Available in an SSOP-20 package, the AS8221 FlexRay transceiver costs $4.20 (1000).
austriamicrosystems, www.austriamicrosystems.com

Touchscreen controller provides small-footprint options

The low-power SX8650 resistive-touchscreen controller provides enhanced ±15-kV electrostatic-discharge protection. The controller supports the 400-kHz, fast-mode I^{2}C serial-bus-data protocol and has a 1.65 to 3.7V operating voltage. Features include a 12-bit ADC for coordinates, touch-pressure measurement, a 50k-sample/sec-throughput output rate, and a 23-μA current consumption at 8k samples/sec. Targeting use in portable and battery-powered, four-wire resistive-touchscreen devices, the platform also suits mobile phones, digital still cameras, MP3 players, personal navigation devices, and handheld gaming devices. In a 3×3-mm DFN-12 package or a 1.46×1.96-mm WLCSP-12 package, the SX8650 platform costs 76 and 78 cents (3000), respectively.
Semtech Corp, www.semtech.com

LIN-bus motor- and relay-control IC suits smart-actuator applications

The MLX81150 automotive-LIN-bus motor- and relay-control IC integrates a physical-layer LIN transceiver, a voltage regulator, and a 16-bit microcontroller with 32-kbyte flash memory. Aiming at smart-actuator applications, the product enables high-voltage I/Os, a timer, an ADC with differential amplifier for current monitoring, a PWM unit, and an EEPROM. The mixed-signal integration of the 0.18-mm process allows for the inclusion of a relay driver, suiting dc-motor applications, such as window lifters, seatbelt retractors, EGR (exhaust-gas-recirculation) flaps, or throttle valves. The device enables direct connection to external power MOS transistors in half- or full-bridge configuration without an additional predriver IC. Using a 4/16-bit dual-task implementation allows the 4-bit task to handle process communication and the 16-bit task to focus on the motor-control algorithm. The LIN-software driver meets the communications tasks of LIN 1.3, LIN2.x, and J2602 protocols. The MLX81150 costs $1.97 (50,000).
Melexis, www.melexis.com

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Burn-in, burn-in: dc inferno

DANIEL VASCONCELLOS

The company I worked for had just finished a rush project to deliver a batch of ruggedized power converters to an integrator that was combining them with ruggedized computers and shipping them out for military use in the first Persian Gulf War, Operation Desert Storm. These power converters would take any standard voltage from 100 to 300V at a frequency of 40 to 400 Hz and a voltage of 28V dc and deliver clean, regulated, 117V, 60-Hz ac with 10 minutes of UPS (uninterruptible-power-supply)-like battery backup at 1500W. We had a commercial product that met this specification, but it was lacking in the ruggedness and environmental specifications that this customer required. We underwent an arduous effort to upgrade the mechanicals and thermal design to meet this customer's requirement. We accomplished this task after about three months of 80-hour weeks.

The most difficult test to pass was the 24-hour test at full load and 85°C. We passed that test on the first attempt and tested 10% of our production run to ensure that we complied. Everything passed, and we shipped all 200 power converters to the integrator. I then took a well-deserved week off.

The customer took all 200 units, attached them to systems, and started a 48-hour burn-in at 70°C. At 36 hours, 100% of the units failed catastrophically. My employer quickly recalled me from my week off and put me on a plane to find out what happened. I found that the primary power bridge in every unit had blown out. There was almost nothing left in the power section that had not melted. I sheepishly returned home with no idea of what had gone wrong. We took our engineering unit and ran it at temperatures as high as 70°C; it, too, failed at 36 hours. There was nothing in the unit that did not reach thermal equilibrium in less than two hours, so how could the unit tell the difference between 24 hours and 36?

It took us two weeks to hunt down the culprit: The output-power stage in our system operated in a patented resonant circuit that used current feedback to keep the output transformer balanced and to fold back to protect from overloading. This current used a digital optocoupler to send pulses back from the power side to the control side. It was one of the parts we had upgraded; it offered 125°C operation and 3500V-ac-rms isolation. We were using it at only 300V dc.

We had assumed that if it was good for 3500V ac, it should be good for 300V dc. With an ac application, no charge migrates across the isolation barrier. Some charge might migrate back and forth, but it changes direction with each ac cycle. When you put a large dc bias across the device, the leakage migrates in only one direction. This leakage increases with temperature. Over time at elevated temperature, charge built up on the receiver side of the device until there was enough charge to affect its operation. It stopped receiving pulses, and the control circuit lost its feedback, driving the output transformer into saturation and emitting smoke.

It turns out that optocouplers for long-term dc use have a screen inside that shunts all of the drifting charge to ground. In short, alternating current and direct current are not interchangeable. It would have been nice if the optocoupler's data sheet had specified "not for dc use."**EDN**

Paul Breed is an engineer at NetBurner Inc (San Diego, CA).

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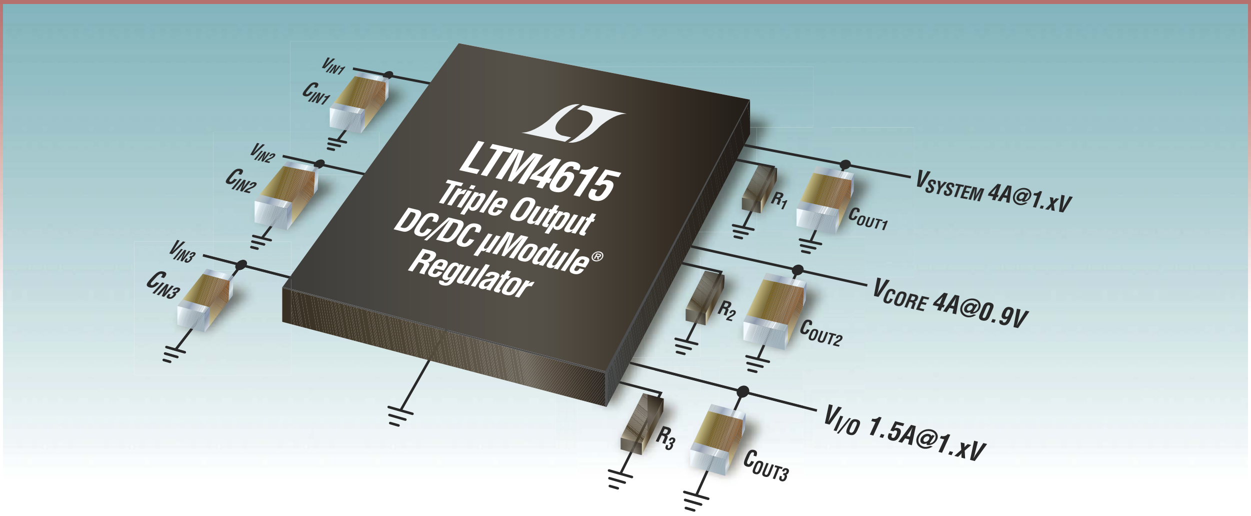

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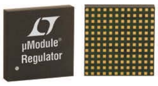
Our new step-down DC/DC µModule regulator family regulates multiple output voltages and operates from common or independent input supplies. Housed in compact LGA packages with integrated inductors, control circuitry, bypass capacitors and power MOSFETs, these µModule regulators reduce bill-of-materials, insertion costs, board space and design time. Simplify your design for powering the latest generation FPGAs, ASICs, DSPs and microcontrollers.

▼ Multiple Output Step-Down DC/DC µModule Regulator Family

Low Voltage: ≤5.5V_{IN}					
Triple	**Output Current Configurations**		**V_{IN} Range**	**V_{OUT} Range**	**LGA (Land Grid Array) Package Size (mm)**
LTM®4615	→ 4A	→ 8A	V_{IN1}: 2.375V to 5.5V	V_{OUT1}: 0.8V to 5V	 15 x 15 x 2.8
	→ 4A		V_{IN2}: 2.375V to 5.5V	V_{OUT2}: 0.8V to 5V	
	→ 1.5A	→ 1.5A	V_{IN3}: 1.14V to 3.5V	V_{OUT3}: 0.4V to 2.6V	
Dual					
LTM4614	→ 4A	→ 8A Also see LTM4608A	V_{IN1}: 2.375V to 5.5V	V_{OUT1}: 0.8V to 5V	
	→ 4A		V_{IN2}: 2.375V to 5.5V	V_{OUT2}: 0.8V to 5V	
LTM4616	→ 8A	→ 16A	V_{IN1}: 2.7V to 5.5V	V_{OUT1}: 0.6V to 5V	
	→ 8A		V_{IN2}: 2.7V to 5.5V	V_{OUT2}: 0.6V to 5V	
High Voltage: ≤26.5V_{IN}					
LTM4619	→ 4A	→ 8A Also see LTM4601A	V_{IN1}: 4.5V to 26.5V	V_{OUT1}: 0.8V to 5V	
	→ 4A		V_{IN2}: 4.5V to 26.5V	V_{OUT2}: 0.8V to 5V	

▼ Info & Free Samples

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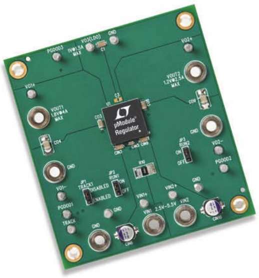

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